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FET GATE DRIVE AND BIPOLAR OUTPUT APPLICABLE TO AHV85110KNHTR GATE DRIVERS

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INTRODUCTION

The increasing speed, voltage, and current in switching power converters has placed increasing demands on FET drivers. Coupled with the increasing popularity of GaN and SiC transistors, operation of the FET driver has become critical to achieving the high performance of these power switches.

Understanding the role and operation of the gate drive loop in a power converter therefore is important in optimizing circuit functionality and avoiding issues that can result from high dV/dt and dI/dt.

This application note explains the turn-on and turn-off procedures of a FET. It also highlights some of the critical parasitic components and how to mitigate their effects, in particular, the use of bipolar drive.

REVIEW OF FET GATE DRIVE

A point worth emphasizing is that it is more important to think in terms of charge transfer rather than simply charging the input capacitance, C_{ISS}, of the FET to turn it on. Furthermore, as shown in Figure 1, FET capacitances are highly non-linear. Capacitance depends largely on the FET V_{DS}.

Figure 1 shows an overview of the voltages and currents in a half-bridge circuit. The detail shows the turn on of the high-side FET. The turn-off procedure is the reverse of the turn-on procedure where charges must be removed from the circuit.

Before time t_0, the circuit conditions are:

- The high-side FET is completed off.
- The low-side FET is off and the inductor current is circulating in the low-side FET body diode.
- For the time scale of the switching transition, the inductor current is considered to be DC.

t_0–t_1

V_{GS_H} begins to rise toward the threshold voltage, V_{TH}, of the FET. The FET remains off and no drain current, I_{DS}, flows.

The high-side FET V_{DS} will be clamped to the supply voltage plus the body diode voltage drop and will remain so until all the inductor current flows in the FET; that is, until the body diode is cut off.

During this period, most of the gate drive current is used to charge the gate-source capacitor, C_{GS}. There is negligible change in the gate-drain capacitor, C_{GD}.

t_1–t_2

At time t_1, $V_{GS\_H} = V_{TH}$ and the FET begins to conduct. I_{DS} begins to rise, but V_{DS} remains clamped by the body diode.

The gate current continues to flow into the C_{GS} and C_{GD} capacitors.

Since V_{DS} is clamped by the body diode to $V_{DD} + V_{BD}$ and V_{GS} is rising toward the plateau level, V_{GP}, the charge during this interval can be estimated as:

$$Q_{GS} \approx \int_{V_{DD}-V_{GP}}^{V_{DD}+V_{BD}} C_{ISS}(V_{DS})dV$$

t_2–t_3

At time t_2, the FET current, I_{DS}, has reached the inductor current level. No current flows in the body diode, so the drain-source voltage, V_{DS}, will begin to fall.

Furthermore, because operation occurs in the saturation region of the FET output characteristic, it can be seen in Figure 1 that the gate-source voltage, V_{GS}, remains constant for a fixed value of I_{DS} for varying V_{DS}. Hence, V_{GS}, is fixed at a plateau level, V_{GP}. This region is the well-documented Miller plateau.

During this period, the gate current is used to charge the gate-drain capacitor, C_{GD}, and the charge required can be estimated as:

$$Q_{GD} \approx \int_0^{V_{DD}} C_{RSS}(V_{DS})dV + \int_0^{V_{GP}} C_{RSS}(V_{GS})dV$$

t_3–t_4

At time t_3, the FET is fully powered-on and enters the Ohmic region of the output characteristic, where the voltage across the FET is determined by the current, I_{DS}, and the on-resistance, R_{DS_ON}.

V_{GS} continues to increase to further enhance the channel until it reaches the supply voltage of the driver, V_{G_DRV}.

HALF-BRIDGE VOLTAGES AND CURRENTS AT A GLANCE

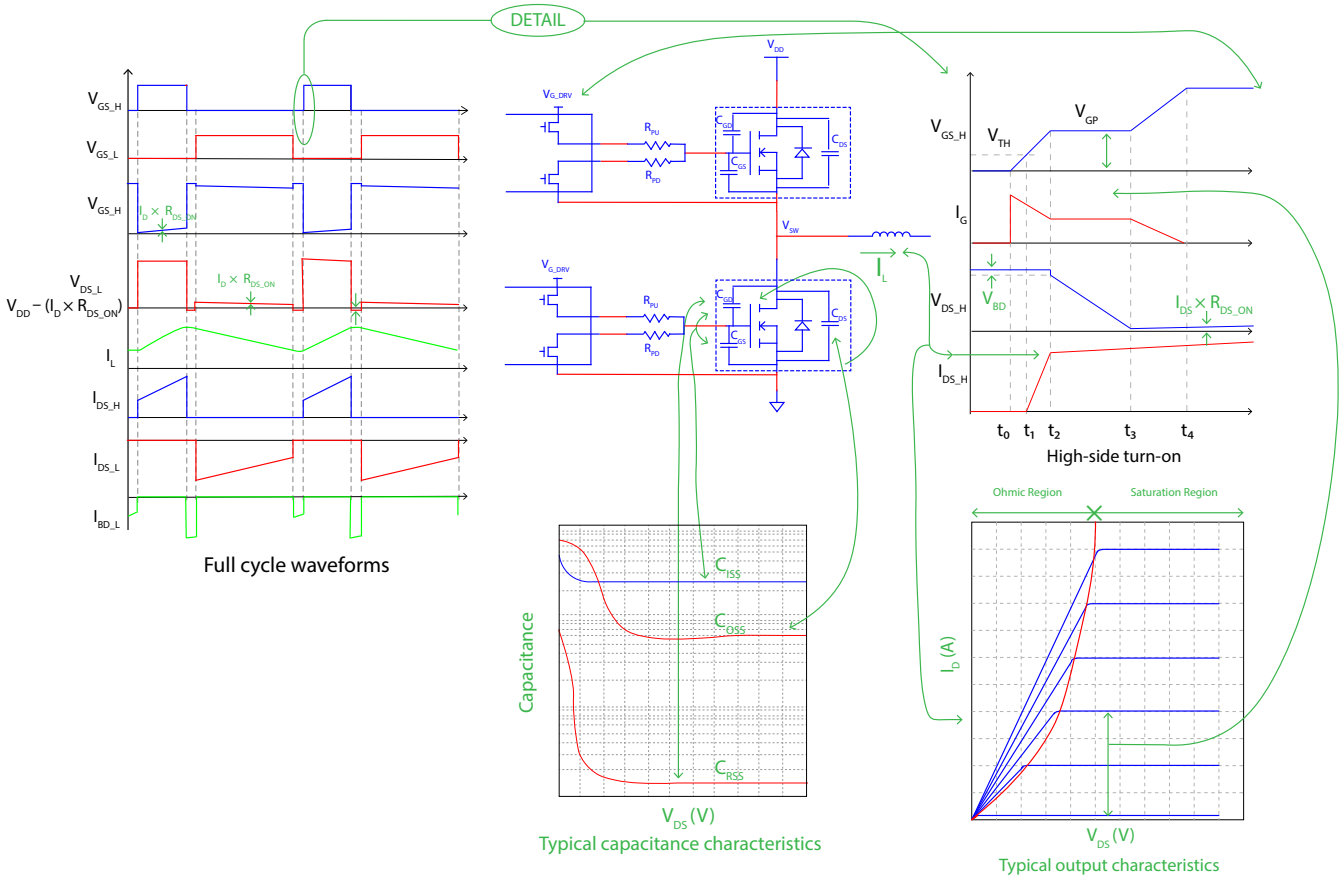

Figure 1: Half-bridge Voltages and Currents

EFFECT OF CIRCUIT PARASITICS ON GATE DRIVE

In any electronic circuit, there are many parasitic components that do not appear on the schematic. FET and IC bond wires and packaging along with PCB traces result in unwanted parasitic inductances. FET internal structures and overlapping PCB traces and power planes add circuit node capacitances.

In most cases, these parasitic components have little or no impact on circuit performance. However, in power switching circuits, they can have a severe effect and should be carefully considered.

The internal structure, packaging, and pinout of the AHV85110KNHTR FET driver have been optimized to minimize such parasitics.

The most effective way to reduce the external circuit parasitics is through good PCB layout. For further details, see application note AN296269, Minimizing PCB Parasitic Effects With Optimum Layout of the Gate Driver Loop.

Figure 2 shows a simple half-bridge power section. This circuit shows the main parasitic components:

- $C_{GS,}$ $C_{GD,}$ and C_{OSS} are the well-documented FET internal capacitances.
- L_G represents the gate driver output including the driver IC package and PCB traces.
- L_{CS} represents the common source inductance; that is, inductance that is shared by the gate drive loop and the power commutation loop. It is made up of FET package inductance and PCB traces. This is the most critical parasitic component and should be minimized through good design and FET choice.
- L_S represents the inductance in the source power loop.
- L_D represents the drain inductance, both FET package and PCB.

FALSE FET TURN ON

The high rate of change of voltages and currents in power switching circuits can create inductor currents and capacitor voltage drops.

One example is the false turn on of a FET due to a dv/dt event. Figure 2 shows the case of the false turn on of the low-side FET. After the low-side FET has been turned off and a suitable dead-time has elapsed, the high-side FET is turned on. This produces a rapidly changing switch node voltage at the drain of the low-side FET. The resulting capacitor current:

$$i_{C_{GD}} = C_{GD} \frac{dV_{DS\_L}}{dt}$$

Flowing in the gate-drain capacitance, C_{GD} and driver output will cause the voltage on the gate of the low-side FET to rise. If this voltage spike peaks beyond the threshold voltage, V_{TH}, the FET will conduct. Because the high-side FET is also conducting, this can result in a potentially destructive shoot-through event.

Furthermore, as shown in the typical FET capacitor characteristics of Figure 1, the capacitors are highly non-linear and a function of V_{DS}. Therefore, the effect of i_{CGD} can be more pronounced at lower values of V_{DS}.

This inevitable i_{CGD} current must be managed correctly and also emphasizes the importance of a strong driver pull down and correct choice of gate resistor. The AHV85110KNHTR driver has independent pull-up and pull-down outputs, allowing independent choice of both resistors.

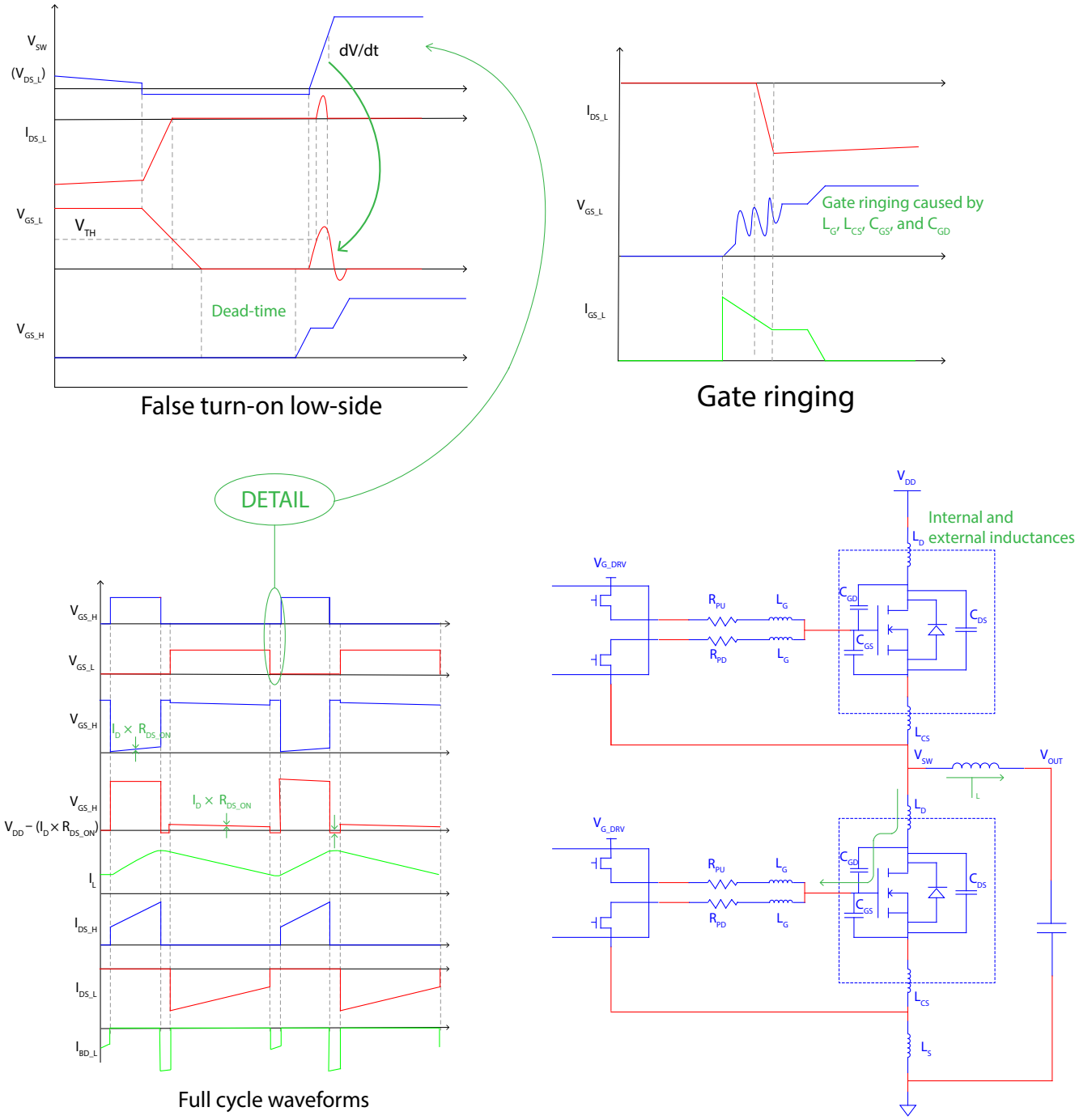

Figure 2: Effect of Circuit Parasitics

Bipolar output drive

A popular method to further mitigate the effects of false turn on is through the use of a bipolar output drive, as shown in Figure 3.

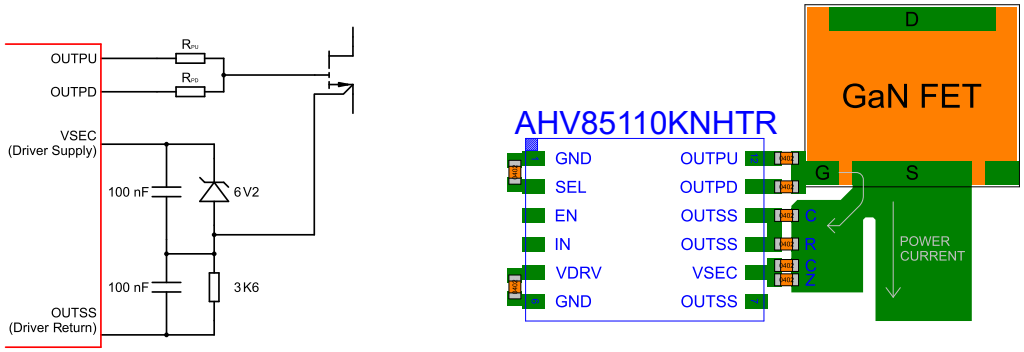

Figure 3: Bipolar Gate Drive

Here, a suitable choice of driver supply voltage, C_{SEC}, and Zener diode generates the $V_{G+} = V_Z$ and $V_{G-} = C_{SEC} - V_Z$ voltages.

As emphasized above, PCB layout is critical for the correct performance of power switching circuits. The AHV85110KNHTR driver pinout easily facilitates this bipolar drive circuit without compromising on the key PCB layout guidelines.

CONCLUSION

Combining new technologies and ever-increasing circuit performance places increasing demand on switching power converter designs. The gate driver is a critical component in these new designs, and an understanding of the detailed operation and second order effects is important. Implementing this knowledge and good design practices will result in optimum gate driver performance facilitating the advantages on new technology power switches.

Revision History

Number	Date	Description	Responsibility
–	August 30, 2022	Initial release	Tyler Hendrigan

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