Monolithic Magnetic Hall Sensor ICs Using Dynamic Quadrature Offset Cancellation

By Alberto Bilotti, Life Senior Member, IEEE, Gerardo Monreal, and Ravi Vig

Abstract—The offset voltage, and its temperature drift and production spread, which generally degrades the zero-level stability and reproducibility of magnetic Hall sensor ICs, can be reduced using a single Hall plate and switching means for periodic permutation of the supply and output contact pairs. The present work describes a chopper-based 5-V monolithic linear Hall sensor IC with a ±0.1 T full scale where this dynamic plate offset cancellation technique has been employed together with a cost-effective signal conditioner. The device was integrated using a 2-µm conventional BiCMOS process and the final chip, measuring 1.5 × 1.5 mm, shows, after packaging in a 3-pin plastic package, a residual offset with a production spread and a temperature-induced drift five to ten times smaller than in currently used multiplate DC quadrature cancellation approaches. The device does not require external components and provides an output free of HF residues.

Index Terms—BiCMOS analog integrated circuits, choppers, Hall devices/effect, microsensors, monolithic integrated circuits.

I. INTRODUCTION

MONOLITHIC magnetic sensor ICs generally use Si Hall elements which are easily integrated with the amplifier or signal-conditioner circuits required for amplification or processing the relatively low voltages generated. The Hall effect, its characteristics, applications, etc., have been extensively dealt with in the literature [1]−[3]. An excellent review with many references can be found in Baltes' and Popovic's work.

The simplest Hall element uses a square plate made, for example, of an Epi-pocket in a bipolar or BiCMOS process with two pairs of orthogonally-oriented contacts, as shown in Fig.1. When a supply voltage V_s is applied across one pair of contacts, for example **a**, **c**, a magnetic flux density B normal to the plate generates a voltage V_H across the other pair **b**, **d**, such that

$$V_H \approx S_v \times B \times V_s \qquad (1)$$

where S_v is the Hall element sensitivity per unit supply voltage. The sensitivity given by $V_H / B \times V_s$ [T^{-1}],

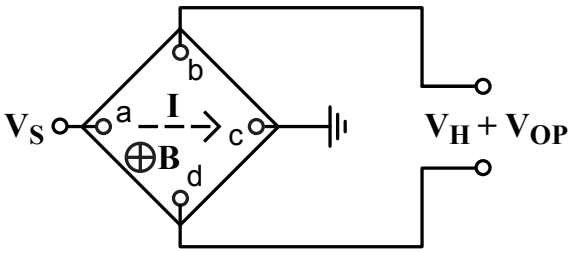

Fig. 1. Basic Hall plate.

where T (tesla; 1 T = 1 × 10^4 gauss) is the meter-kilogram-second (mks) unit for magnetic flux density (induction), is approximately a constant parameter, depending only on the Si layer mobility and the plate and contact geometries. Typical values of S_v range between 0.04 and 0.08 T^{-1}, which means, for a typical 5-V supply and minimum magnetic flux density of 1 mT, output voltages of 200 to 400 µV.

In all DC applications, the minimum magnetic flux density capable of being accurately measured by such plates depends on the offset voltage V_{op} appearing at the plate output contacts for $B = 0$. The plate, from an electrical point of view, will show unavoidable imbalances due to resistance gradients, geometrical asymmetries [4], piezoresistive effects [5], [6], etc., generating a nonnegligible offset voltage. As the plate offset V_{op} is relatively large—it may range from 0.5 to 5 mV for a 5-V supply and is temperature-, supply voltage-, and stress-dependent—efforts have been made for cancelling or minimizing its effects.

Offset cancellation cannot be performed by such switching techniques as those used in amplifiers, as there is no available state where V_{op} could be isolated from V_H except cutting off the magnetic field, which is certainly a nonviable proposal.

Noting that, from a DC point of view, the Hall plate can be viewed as a distributed resistive Wheatstone bridge, most

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present commercial Hall sensor ICs cancel the offset by using two or more appropriately interconnected plates where the electrical current direction is 90° rotated from one plate to the other [7]. If the imbalance source remains invariant and fixed in the solid space, the offsets of any pair of plates will be equal but of opposite polarity, achieving the desired cancellation. On the other hand, the useful signal of the multiplate arrangement remains equal to that of a single plate.

Alternatively, the use of only one plate while generating the quadrature states by periodic supply and output contact permutations has been proposed [8], [9]. Although this *dynamic offset cancellation technique* requires a more complicated signal conditioner following the Hall switched-plate, it has the advantage of reducing the residual offset and its production spread as compared with multiplate sensor ICs. In the last case, the zero-level deviations are degraded due to plate offset mismatches between physically different plates, these mismatches being mostly generated by the plastic package temperature-dependent built-in stresses.

This work describes 5-V BiCMOS monolithic linear Hall sensor ICs using the dynamic offset cancellation technique, where the various functions required for recovering the useful signal and cancelling the offset are performed by a cost-effective signal conditioner.

A BiCMOS technology was preferred in order to have simple high-gain open-loop amplifiers with low offset, accurate temperature-programming circuits, as well as a low-cost high-output current sourcing capability.

II. THE SWITCHED HALL PLATE

The simplest dynamic offset cancellation technique uses a single square plate with four contacts where the quadrature states are generated by periodically connecting the supply voltage and supply conditioner input to one pair of contacts or to the other, as shown in Fig. 2. Each state, which we shall call from now on the *0° state* or the *90° state*, is defined by the complementary clocks CLK1 and $\overline{\text{CLK1}}$, respectively.

Assuming $B = 0$ and an ideal Wheatstone bridge model for the Hall plate, the voltages appearing at the output contacts are the plate offsets $V_{op}(0°)$ and $V_{op}(90°)$ which are equal in magnitude but have opposite polarities. This can be verified in a very simple way as follows. Assume that an imbalance, for example due to a stress pattern, occurs such that the region between contacts **a** and **b** shows a resistivity smaller than the rest of the plate (dotted resistor in Fig. 2), and that this situation does not change when changing states. Then, the offsets developed at each state have the same magnitude but opposite polarities, as the same imbalance occurs in adjacent branches of the equivalent bridge network (the Hi terminal will be more positive than the Lo terminal in the 0° state but more negative in the 90° state).

For $B \neq 0$, as the supply and output connections rotate in the same direction, V_H keeps its polarity unchanged, making V_H invariant. This characteristic of V_H derives from the antireciprocal property of a symmetrical Hall plate.

There appears, therefore, a simple way to discriminate the offset from the useful signal and further cancelling the offset by appropriate signal conditioning. Although in Fig. 2, V_H is quasi-constant and V_{op} an alternating square wave, waveforms can be interchanged if desired by interchanging output contacts **a** and **c** during the 90° state.

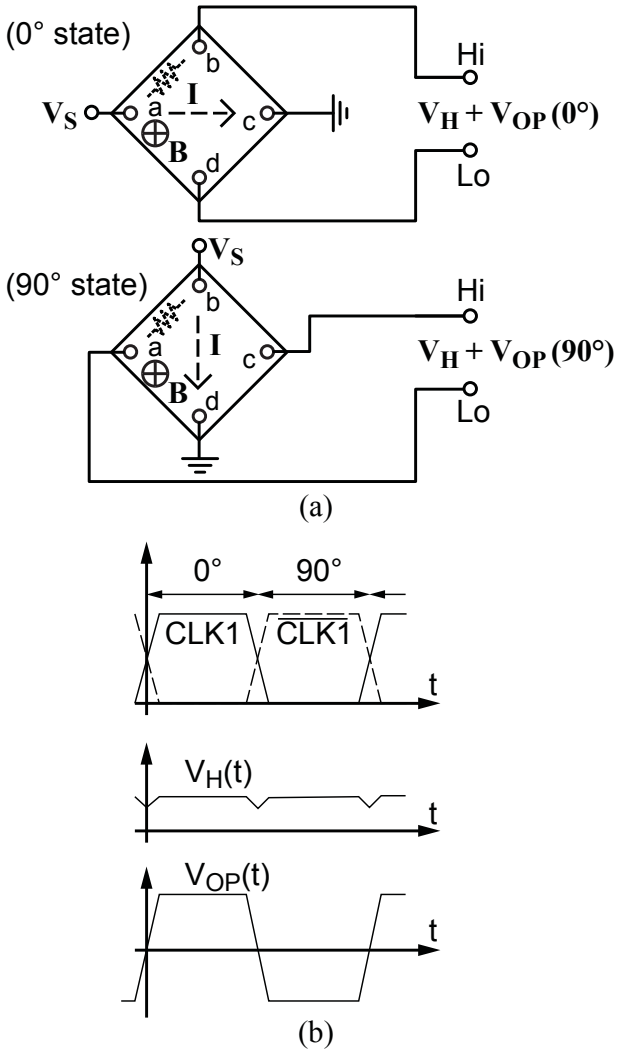

Fig. 2. (a) In a dynamic offset cancellation technique, the current flowing through the plate is periodically switched from the 0° to the 90° direction and vice versa. (b) Clock, Hall voltage, and plate offset waveforms.

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As an ideally perfect cancellation is never possible, there is in practice a residual plate offset $V_{op}(r)$ defined as

$$V_{op}(r) = |\, V_{op}(0°)| - |\, V_{op}(90°)| \qquad (2)$$

where absolute values have been preferred for emphasizing the polarity reversals occurring during further signal processing. Depending on the fabrication process, the Hall plate geometry and crystallographic orientation, and the residual wafer and package stresses, $V_{op}(r)$ may range between 50 and 500 µV for a 5-V supply.

DC measurement data of a quadrature cancellation on a single plate, either in an Epi plate [9] or in an MOS channel "plate" [10], showed an appreciable improvement as compared to the conventional multiplate approach. For reducing $V_{op}(r)$ these measurements were performed in plates using four pairs of contacts distributed around the periphery of a circular plate as in a "spinning" Hall cell [9]. In this case, multiplexed addition of all possible offsets for improving cancellation would require eight switching states per cycle.

For simplifying purposes and reducing chip area, the simplest approach of the Epi plate with two pairs of contacts and two phases per cycle as shown in Fig. 2 was chosen for our monolithic sensor IC.

The maximum allowable plate switching frequency depends on the plate voltage settling time after each commutation transition. Note that, for example, after the transition from the 0° state to the 90° state, the voltage V_a at contact **a** in Fig. 2 has to decay from V_s to $V_s/2$, and V_c has to increase from zero to $V_s/2$ (while voltages at **d** and **b** have to decay to ground and increase to V_s, respectively). This requires a rearrangement of charges stored in the Epi-Sub reversed-biased junction and therefore, a certain time for voltages to settle down into the final value $V_s/2$, after which the Hall output voltage will be valid and ready to be processed, as shown in Fig. 3.

Switching measurements, of a Hall plate built on a square Epi layer that was 2 Ω-cm, 5.5 µm thick, with 3 kΩ resistance between diagonal-opposite facing contacts, showed that the Hall voltage will be valid only after ≈600 ns have elapsed from the plate commutation transition. Taking into account component tolerances and the fact that additional sample pulses must be included in each phase, a maximum plate switching frequency of 200 kHz was found. As long as the switching frequency remains below this limit, the switching frequency is not critical for the system operation, simplifying, therefore, the implementation of the clock circuitry.

Even if there would be a residual voltage due to an excessive settling time, this voltage would remain invariant during both states, just as the true offset does, and therefore would be cancelled out. This has not been exploited further as it requires a very accurate and more costly CLK generator.

Fig. 4 shows the actual switched-plate arrangement used in the monolithic sensor IC where the four single-pole double-throw (SPDT) switches required for the contact permutation were implemented with MOS transistors. The plate contact interconnections follow the basic scheme of Fig. 2 except for an inter-

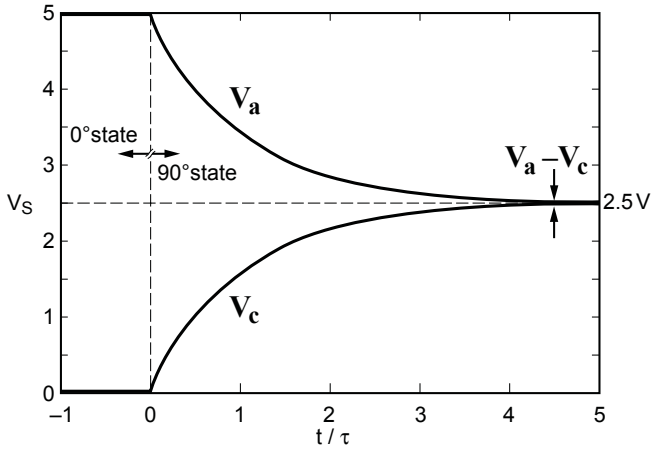

Fig. 3. 0° state to 90° state Hall plate switching transient where V_a and V_c are the voltages at contacts **a** and **c** in Fig.2.

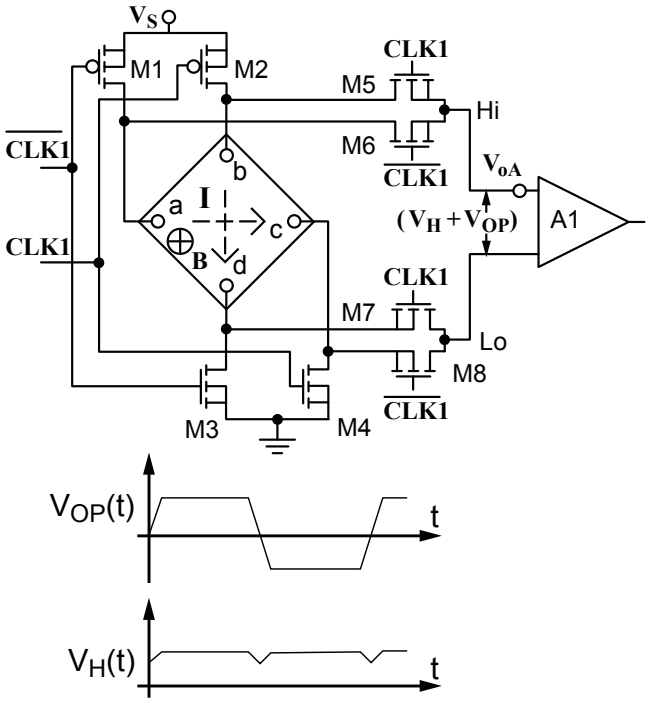

Fig. 4. Switched Hall Plate. When the *CLK1* signal is high, current flows between **a** and **c** (0° state) and when $\overline{CLK1}$ is high, current flows between **b** and **d** (90° state).

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change of the output terminals during the 90° state. With this arrangement, at each change of state, V_H changes polarity and V_{op} remains quasi-constant, in such a way that V_{oA}, the DC input-referred offset of amplifier A1, will become indistinguishable from V_{op}, and the Hall plate and the input amplifier offsets will be simultaneously processed and cancelled by the signal conditioner.

Thus, the A1 offset is cancelled at no cost, avoiding the extra hardware required to perform the same function by other techniques such as autozero, signal conditioning (SC), etc.

The input voltages to the ideal amplifier A1 become

$$V_i\,(0°) = V_H + |V_{op}\,(0°)| + |V_{oA}\,| \text{ during } 0° \text{ state} \quad (3a)$$

$$V_i\,(90°) = -V_H + |V_{op}\,(90°)| + |V_{oA}\,| \text{ during } 90° \text{ state.} \quad (3b)$$

For avoiding degrading $V_{op}(r)$ through eventual mismatchings between the supply voltages effectively applied to the plate during each phase, transistors M1 through M4 were properly sized so as to keep their on-voltage drop below 100 mV.

Taking into account that the total offset $V_{op} + V_{oA}$ must be amplified without distortion by A1, dynamic range considerations require minimizing V_{oA}, therefore suggesting the use of a low-offset differential bipolar input stage. In this case, base input currents I_b flowing through MOS switches M5 through M8 may generate a residual offset $V_{oI}(r)$ additional to that given by equation 2. Assuming $\Delta I_b \ll I_b$, straightforward calculation gives

$$V_{oI}(r) = \Delta R_{ch} \times I_b \quad (4)$$

where

$$\Delta R_{ch} = R_{ch}(\text{M5}) + R_{ch}(\text{M8}) - [R_{ch}(\text{M6}) + R_{ch}(\text{M7})]\ . \quad (5)$$

As A1 uses a conventional base current cancellation circuitry, $V_{oI}(r)$ is smaller than 2 µV and, therefore, can be fully neglected as compared to $V_{op}(r)$.

III. SIGNAL CONDITIONER

Fig. 5 is a simplified block diagram of the complete linear Hall device, where the previously described switched-Hall plate is represented by block SWP. Note that for zero offset and $B = 0$, the output amplifier A2 has its quiescent output voltage, V_{Qoi}, defining the sensor zero level, at $V_s/2$. The signal conditioner operates as a quasi-chopped amplifier where the first pair of cross-coupled switches are built in the switched Hall plate, and where the second pair of switches plus the conventional low-pass (LP) filter have been substituted by sample and hold (S/H) and adding functions, as described next.

The differential-differential amplifier A1 amplifies G1 times the signal V_i comprising the quasi-DC offset voltage plus the alternating useful Hall signal generated by the switched Hall plate. In conventional chopper amplifiers, the useful signal is recovered and the offset cancelled by additional switches after the amplifier, that inverts again the composite signal polarity, and by further LP filtering.

In this application, as at low magnetic flux density levels, the V_{op}/V_H ratio may attain high values, a costly multiple-pole LP filter is required for reducing the residual AC ripple. For example, for insuring a maximum peak-to-peak ripple of 20% in the worst case of V_{op} = 10 mV and V_H = 0.25 mV, the fundamental component of the square-shaped offset voltage must be attenuated 52 dB. When operating at a clock frequency of 150 kHz with a bandwidth of 34 kHz, a four-pole LP filter is required. Besides, the useful signal may be corrupted by DC components, generated by the large pulses occurring at each plate switching, that may go through the LP filter.

The problem was circumvented by using, at the outputs of A1, two S/H circuits S1 and S2, which are clocked by narrow pulses *CLK2(0°)* and *CLK2(90°)*, respectively. This occurred during the 0° and 90° states, once the required delay for the plate commutation transients to die out had elapsed [11].

Assuming an ideal S/H function, the offset voltages at the S/H outputs are DC signals, and there is no need any more to further filter out the otherwise high offset AC ripple, relaxing the output LP filtering requirements. Also, the synchronous sampling of the

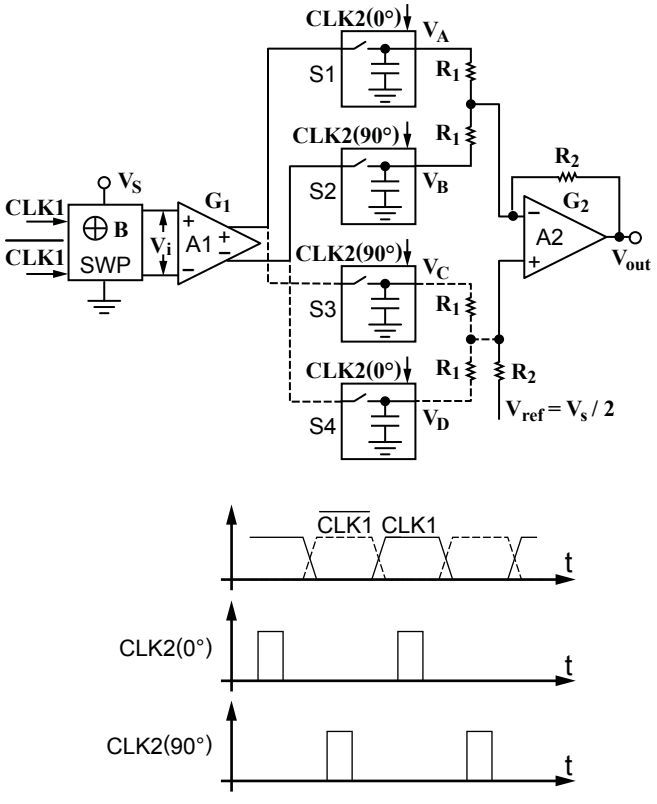

Fig. 5. Hall device block diagram.

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signal by the samplers when the signal is free of spurious pulses improves the accuracy of the signal recovery process, particularly at low levels.

As far as the output noise is concerned, this is mainly due to the thermal noise of the Hall plate resistance. When compared to a conventional chopper, the S/H function in the present approach produces a higher noise power spectral density at low frequencies due to a higher "fold-back" of HF noise components into the baseband.

Recalling equations 3a and 3b, assuming ideal S/H functions and noting that the S/H inputs are complementary outputs of A1, the S/H outputs V_A and V_B are, neglecting common mode (CM) signals, DC voltages given by

$$V_A = ½G_1 \, [V_H + |V_{op}\,(0°)| + |V_{oA}\,|\,] \tag{6}$$

$$V_B = ½G_1 \, [V_H - |V_{op}\,(90°)| - |V_{oA}\,|\,]. \tag{7}$$

Adding these two DC voltages, by means of the inverting two-input summing op-amp A2, with gain $G_2 = -R_2/R_1$, and then inserting the quiescent output voltage V_{Qo}, produces, neglecting A2 offset contributions, the output

$$\begin{aligned} V_{out} &= V_{Qoi} + G_2\,(V_A + V_B\,) \\ &= V_{Qoi} + ½G_1 \times G_2 \times V_{op}(r) + G_1 \times G_2 \times V_H \end{aligned} \tag{8a}$$

or

$$V_{out} = V_{Qoi} + G_1 \times G_2 \times V_H \tag{8b}$$

where $V_{Qoi} = V_{ref} = V_s/2$ is the ideal quiescent output voltage for $V_{op}(r) = 0$ and V_{Qo} the actual quiescent output voltage. Note that the amplification $½G_1 \times G_2$ of the undesirable residual offset is half that of the useful signal.

Apart from $V_{op}(r)$, there are other components that remain uncancelled and that will shift V_{Qo} from its ideal value, such as offsets due to the feedback amplifier, resistor networks, and S/H mismatchings, etc. As the total offset can be nulled at one temperature by any wafer-trimming technique, the offset drift with temperature and its production spread, particularly due to package-induced stresses, remain the most critical sensor IC issues.

For reducing the effects of S/H imperfections such as charge feedthrough, droop, nonlinearity, etc., the final monolithic sensor IC uses a fully differential S/H configuration comprising four S/H circuits S1 to S4 and a summing feedback difference output amplifier, as shown with dotted lines in Fig.5. In this way, the signal is differentially processed all along the whole system.

Amplifier A1 is an open-loop amplifier with a bipolar input differential stage using differential resistive loads, as shown in Fig. 6. The quiescent output voltage is stabilized by means of a negative feedback loop comprising Q5, Q6, M5, M6, and M7. As compared to a closed-loop amplifier, the open-loop approach does not require stability capacitors, avoiding any settling time degradation due to slew rate limitations.

Care was exercised to avoid undesirable saturation effects increasing the amplifier settling time beyond the plate settling time previously discussed, decreasing the maximum allowable switching frequency. For this, a gain-killer circuit comprising a simple gated CMOS pass transistor that short-circuits the bases of Q7 and Q8 during the Hall plate switching transitions was incorporated into the amplifier.

Although maximum gain is a desirable feature for reducing the effect of post-amplifier offsets as compared to $V_{op}(r)$, the input stage was emitter-degenerated for increasing the linear input

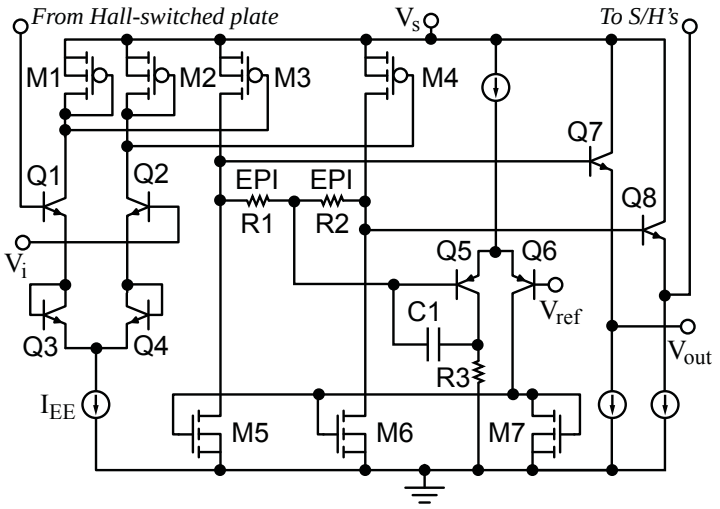

Fig. 6. First amplifier A1.

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range. The linearity, for the maximum input swing, is better than 99.9%.

Diodes were used for emitter degeneration for keeping the stage transconductance proportional to I_{EE}/V_t, allowing simple linear adjustment of I_{EE}. By using a PTAT (proportional to absolute temperature) emitter current bias, the stage transconductance becomes temperature independent, while the Epi load resistors, similar to the Epi plate, make the amplifier gain vary with temperature as $(\text{mobility})^{-1}$ cancelling the Hall sensitivity mobility dependance and reducing the sensor IC sensitivity variations with temperature.

In any chopping amplifier the higher the chopping frequency the smaller the filter capacitors. Consequently, for reducing the chip area, a chopping frequency of 170 kHz, close to the maximum allowed by the Hall plate transition times, was chosen.

The amplifier has a typical gain of 30×, a –3 dB frequency of 4 MHz, and a 0.01% settling time of 400 ns. The offset square wave signal is therefore amplified with negligible frequency distortion.

The S/H function is performed at signal levels G_1 times higher than the input level, making the undesirable effects of S/H imperfections less noticeable, these imperfections being further cancelled by the differential S/H arrangement previously mentioned.

For cost-reduction purposes, the S/H elements were implemented as open-loop circuits, the grounded holding capacitor being sensed by a high-beta lateral-PNP (LPNP) bipolar transistor, Q3 as shown in Fig. 7. Transistors Q1, Q2, and Q4 help reducing Q3 base current, reducing therefore the droop.

The output rail-to-rail feedback amplifier is a rather conventional op-amp. It has a typical gain of 6× and is capable of sourcing a maximum of 2 mA into the load. An internal feedback capacitor of 20 pF stabilizes the loop and limits the bandwidth to ≈30 kHz. This post-sampling narrowbanding reduces the typical output staircase ripple at high operating frequencies and the output white noise.

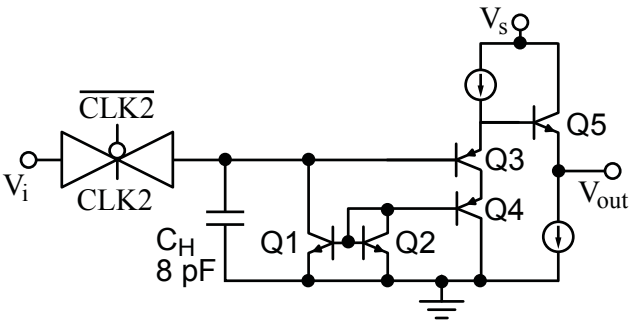

Fig. 7. S/H circuit configuration.

IV. MONOLITHIC IMPLEMENTATION

A ±0.1 T full scale linear Hall device using dynamic offset cancellation and the basic circuits previously described was implemented in a monolithic IC using a 2–µm BiCMOS process. The supply voltage is 5 V ±10%, and no internal voltage regulator is used because in many applications of linear sensor ICs, particularly in the automotive environment, the sensitivity should preferably be proportional to the supply voltage. This ratiometric feature allows cascading the sensor IC output directly to an A-to-D converter fed from the same supply. The device uses no external components, is packaged in a 3–pin plastic package, and operates within a –40°C to 150°C temperature range.

In order to reduce the production spread of the magnetic sensitivity, gain G_1 is trimmed by adjusting I_{EE} (Fig. 6) with a 4-bit binary-weighted fuse-link network. Similarly, the total circuit residual offset, affecting the quiescent output voltage, is trimmed out by another fuse-link network. Both adjustments are performed at the wafer level at one single reference temperature.

The chip, measuring 1.5 × 1.5 mm, is shown in Fig. 8. The Hall Epi plate, measuring 160 × 160 µm, is located at the chip geometric center. The three clock signals *CLK1*, *CLK2(0°)*, and *CLK2(90°)* are derived from a master oscillator, and are generated on-chip.

As low-level analog and 5-V digital signals share the same chip, layout precautions were taken for minimizing digital feedthrough into sensitive areas, therefore minimizing any residual output digital noise.

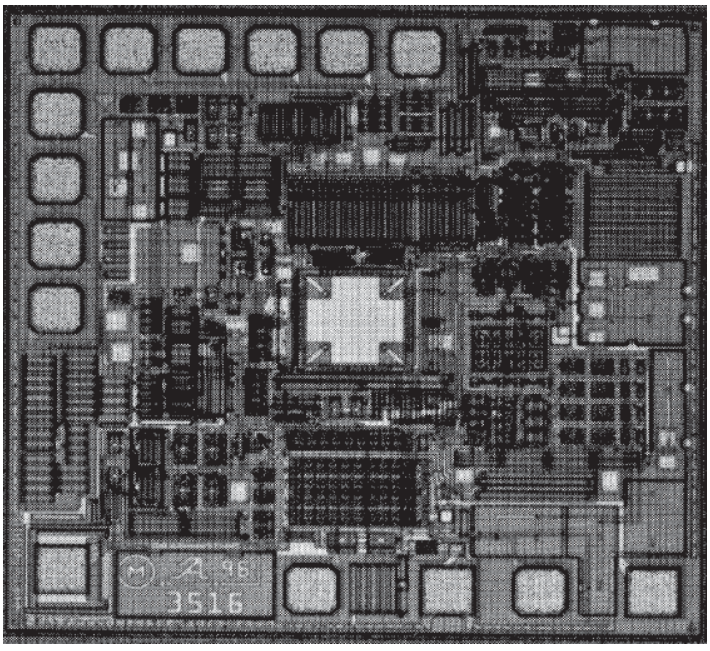

Fig. 8. Microphotograph of the Hall sensor IC die. Die size is 1.5 × 1.5 mm.

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V. EXPERIMENTAL RESULTS

Table I gives the measured typical characteristics of the final packaged Hall device at T_A = 25°C.

TABLE I

V_{supply}	5 V
I_{supply}	7 mA
I_{out}(max)	2 mA
Sensitivity	25 V/T
Full scale	±100 mT
Quiescent output voltage	2.5 V
Equivalent magnetic offset	0.5 mT
Linearity	99.9%
Output noise*	1 mVrms
Bandwidth	30 kHz

*V_{supply} lead decoupled with a 0.1 µF capacitor.

Fig. 9 shows the measured Hall device transfer function $V_{out} = f(B)$. The linearity, measured as an approximation to the best fit to an ideal straight line, amounts to 99.9%.

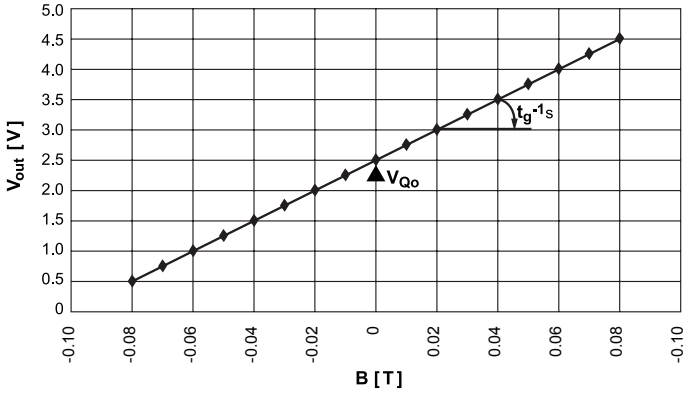

Fig. 9. Measured transfer function Vout = f(B) at 25°C.

Figs. 10 and 11 show the performance of VQo, and total sensitivity S, as functions of temperature within the full ambient temperature range –40°C to 150°C.

The total output residual offset can be derived by measuring the difference between VQo and Vref (see Fig. 5) at the wafer level. Measurements at 25°C show offsets ranging from 5 to 20 mV, i.e., from 0.2 to 0.8 mT. The 2.5-V wafer-trimmed value of VQo at 25°C remains practically unchanged after packaging. The VQo deviation at other temperatures from its reference value at 25°C, shown in Fig. 10, represents a temperature-induced drift in the offset voltage. The typical total drift for the full temperature range is ≈7 mV, equivalent to a magnetic field of ≈0.3 mT. Preliminary production data show a 3σ spread in the quiescent output voltage of only ±10 mV. When using multiplate static offset cancellation techniques, these deviations, mainly caused by package-induced stresses, can be much larger, degrading the sensor IC zero reference stability.

Fig. 12 shows the sensitivity variation with the supply voltage.

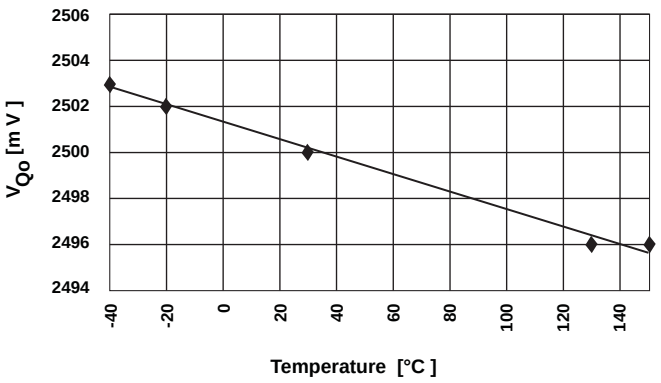

Fig. 10. Typical quiescent output voltage variation with temperature.

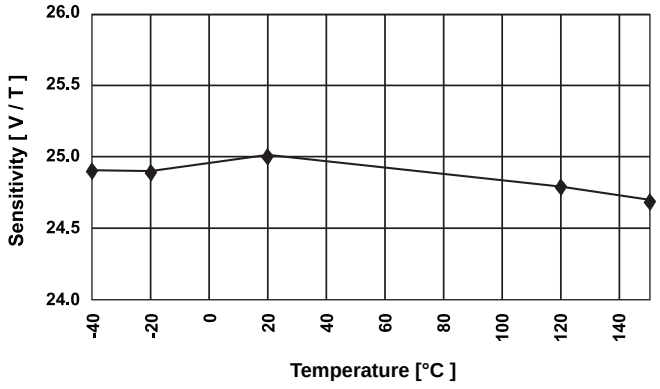

Fig. 11. Typical sensitivity variation with temperature.

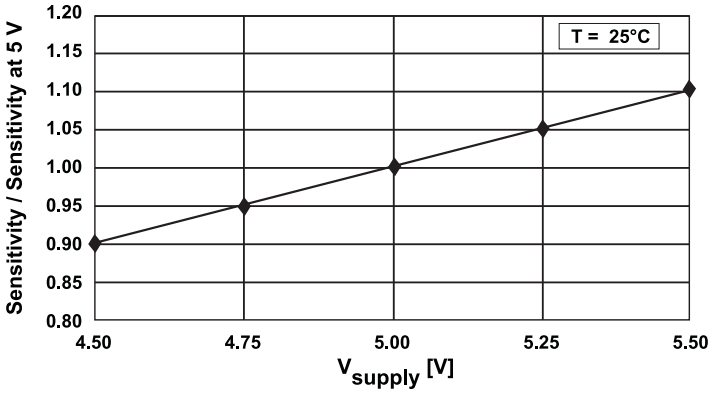

Fig. 12. Typical sensitivity variation with supply voltage.

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Fig. 13 gives the Hall device output for $B = 0$, the oscilloscope photo being taken with the timebase synchronized to the clock frequency. It shows that due to the on-chip S/H filtering action, the CLK frequency residue is negligible and the main HF components left at the output are only those due to the random noise generated by the Hall plate resistance. Consequently, no external LP filter is required. If desired, the output noise can be further reduced by additional external LP filtering at the output, reducing at the same time the system bandwidth.

Finally, Fig. 14 shows the sensor IC output voltage for a sinusoidal magnetic flux density.

VI. CONCLUSIONS

The described ±0.1 T monolithic Hall linear sensor IC using dynamic switching with two pairs of contacts and two switching states appears to be an attractive cost-effective option for reducing the sensor IC offset drift with temperature and the offset reproducibility. As the offset itself is easily trimmed out at the wafer level at one reference temperature, the offset drift with temperature and its reproducibility particularly in plastic-packaged devices becomes the most crucial issue affecting the sensor IC zero stability. In this respect, the present device, after plastic packaging, shows a zero-level stability that compares very favorably with commonly used multiplate DC approaches.

The relatively small chip size proves that this technique can be cost-effective, particularly when recovery of the useful signal and offset cancellation are performed by S/H circuits, substituting for the large-footprint LP filter of a conventional chopper used otherwise. The S/H circuits also help in ignoring the large commutation transients occurring during plate switching, providing an accurate and smooth linear transfer function at very low levels.

Although digital and low-level analog signals share the same chip, the spurious CLK noise developed at the output is almost negligible as compared to the random noise due to the Hall plate resistance.

As suggested in the literature, a higher number of plate contact pairs and switching phases per cycle seems to improve the Hall plate offset cancellation. Certainly this option could be an interesting challenge, requiring a more refined signal-conditioning circuitry operating at higher frequencies and showing an offset sufficiently small not to compromise the advantages gained by the more sophisticated plate switching.

Although the present work deals with linear Hall sensor ICs, the same techniques could be used for implementing the commonly used digital sensor ICs with “operate” and “release” switching levels. In this case, the improvements in the zero level deviations achieved in the present linear sensor ICs will translate into better reproducibility and temperature stability of the switching thresholds.

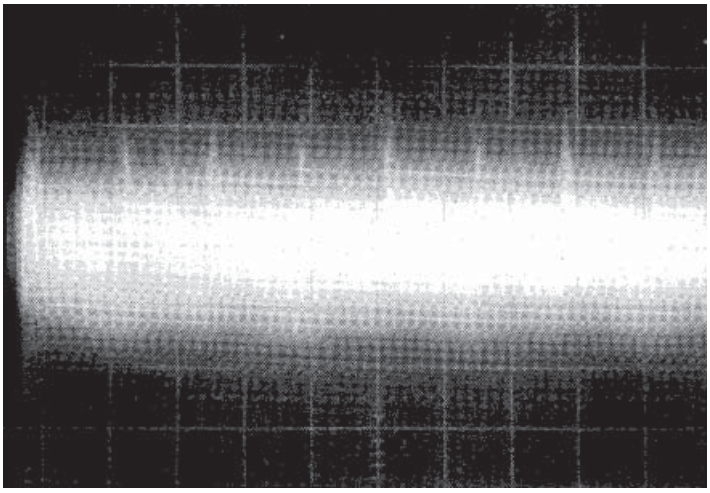

Fig. 13. System output noise, measured with a 0.1 µF decoupling capacitor at the V_{supply} lead. Vertical sensitivity 2 mV/div. Horizontal sensitivity 1 µs/div. Timebase synchronized to CLK frequency.

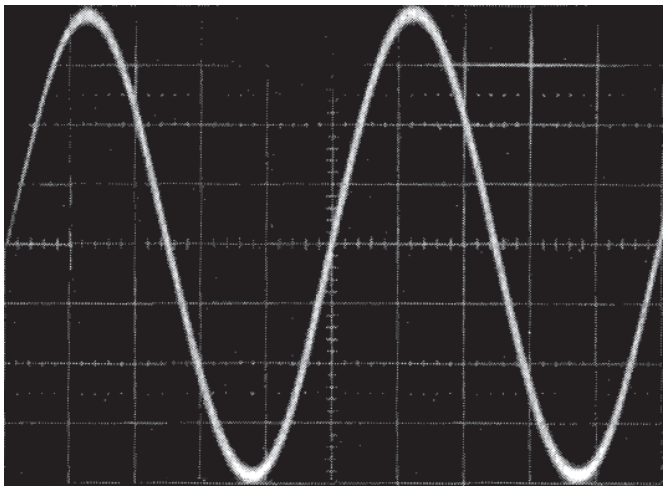

Fig. 14. Output waveform for a 400 Hz sinusoidal magnetic flux density. Vertical sensitivity 50 mV/div. Horizontal sensitivity 0.5 ms/div. Magnetic flux density amplitude: 8 mT.

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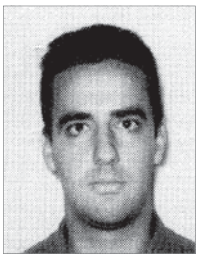

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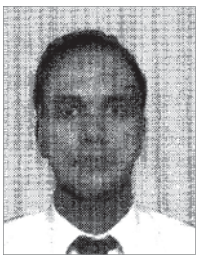

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