Programming Guide

Introduction

This ACS37600 programming guide details the communications interface, memory map, programming protocol, and examples. The guide is designed to be used as a complement to the ACS37600 datasheet which details device specifications and functionality.

The Allegro ACS37600 current sensor IC is a highly customizable solution for multiple applications in AC and DC current sensing. Programmable sensitivity, reference voltage, and overcurrent fault detection enables flexibility over a broad range of industrial, commercial, and consumer applications.

Serial Communication

The serial interface allows an external controller to read and write device EEPROM using bidirectional Manchester communication via the VREF pin. The ACS37600 does not initiate communication; it only responds to commands from the external controller. Each transaction consists of a command from the controller. If the command is a write, there is no acknowledgment from the device. If the command is a read, the device responds by transmitting the requested data.

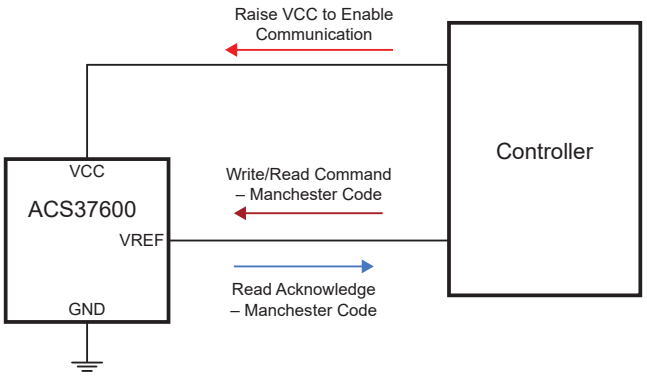

Figure 1: Programming Connections

The serial interface uses a Manchester-encoding-based protocol per G.E. Thomas (0 = rising edge, 1 = falling edge), with address and data transmitted MSB first. The ACS37600 recognizes the following commands: Write Access Code, Write to Non-Volatile Memory (EEPROM), and Read. One frame type, Read Acknowledge, is sent by the device in response to a Read command.

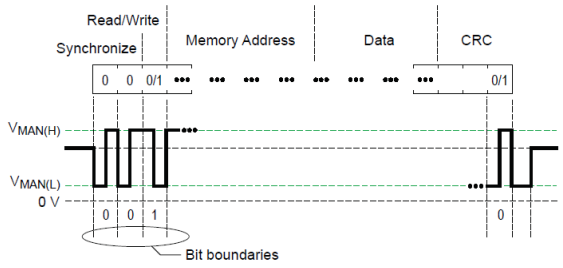

Figure 2: General Format for Serial Interface Communication

Programming Guidelines

Initiating Communications

The controller must open the serial communication with the ACS37600 by performing a memory unlock sequence. This sequence requires the writing of an access code to the access register at address 0x26 and must be completed following power up within the constraints of timers TO1 (20 ms) and TO2 (2 ms) or the device will be disabled for read and write access. The TO2 timer is only activated when UNLOCK_CODE = 1. The user access code is applied by writing register 0x26 = 0x2C413736.

There are two built in memory locking functions that can be implemented in conjunction with the access code:

1. When the ANALOG_LOCK bit is set to 1, (register 0x0F[24]), then V_{CC} must be pulled above $V_{OVD(H)}$ (8 V) to override an internal memory access lock. Once $V_{CC} > V_{OVD(H)}$, the VREF output is placed in a high-impedance state and can easily be driven by a controller. When ANALOG_LOCK = 0, the VREF pin can be overdriven without pulling $V_{CC} > V_{OVD(H)}$. When ANALOG_LOCK = 0, the VREF overdrive requirements are as follows:

VREF Source Current, VREF to GND	1 mA
VREF Sink Current, VREF to VCC	10 mA

2. When the UNLOCK_CODE bit is set to 1, (register 0x0F[25]), then every communication needs to start with the unlock code prior to the access code. The unlock code is applied by writing register 0x26 = 0xAFCF6C27.

The ACS37600 defaults with ANALOG_LOCK = 0 and UNLOCK_CODE = 0 to provide ease of programming at end-of-line calibration. Once calibration is complete, it is strongly recommended that ANALOG_LOCK and UNLOCK_CODE be set to 1 to lock the memory and ensure against accidental programming in the field.

The start of any Manchester command should begin by driving VREF low for at least 2 ms to ensure reset of the Manchester state machine. If a valid unlock sequence hasn't been completed before timeout TO1 expires, VREF will resume normal operation and the device memory remains locked for communications until a power reset occurs. Additionally, after three failed attempts to unlock the memory, the device is locked until the next power-cycle. Figure 3 shows a flowchart of the communications initialization sequence. Figure 4 shows the timing diagram for the initialization sequence required for memory access when ANALOG_LOCK = 0 and UNLOCK_CODE = 0. Figure 5 shows the timing diagram for the initialization sequence required for memory access when ANALOG_LOCK = 1 and UNLOCK_CODE = 1.

Once the memory is unlocked at power-up, it can be accessed at any point while the device remains powered. Figure 6 and Figure 7 show the timing diagrams for EEPROM access when ANALOG_LOCK = 0 and ANALOG_LOCK = 1, respectively. The full memory map available to the user is shown in Table 3, Table 4, and Table 5.

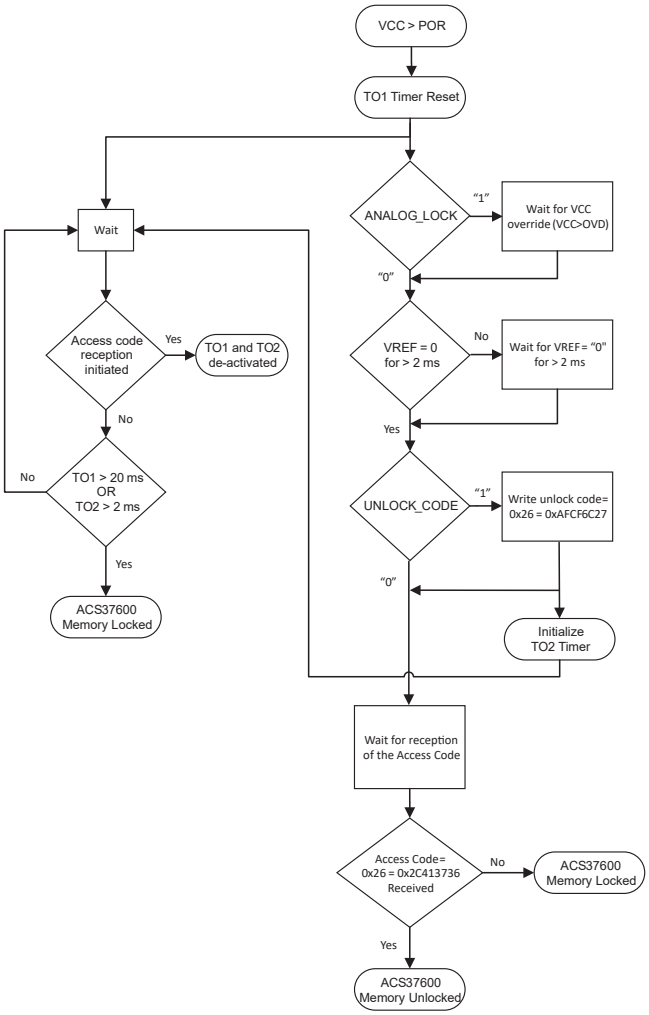

Figure 3: Communications Initialization Sequence Flowchart

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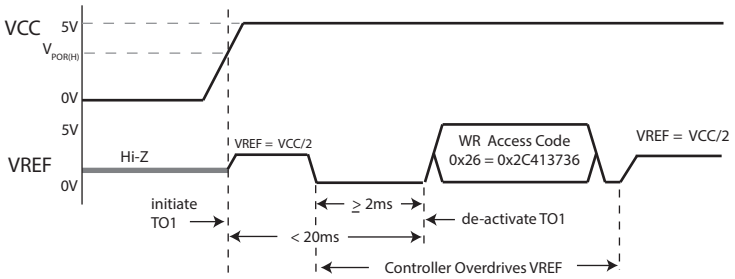

Figure 4: Communications Initialization Sequence with ANALOG_LOCK = 0, UNLOCK_CODE = 0

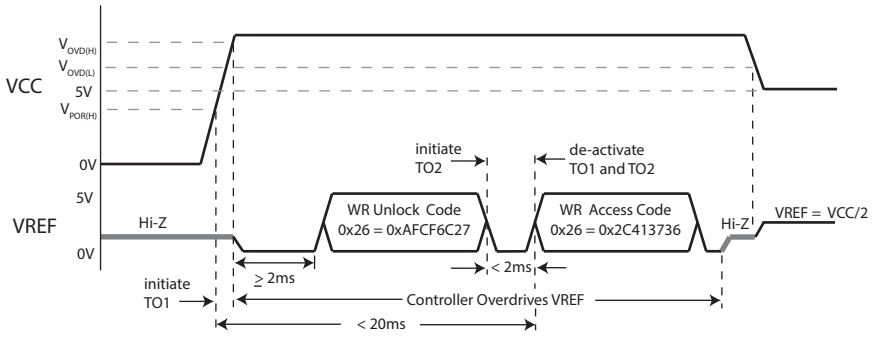

Figure 5: Communications Initialization Sequence with ANALOG_LOCK = 1, UNLOCK_CODE = 1

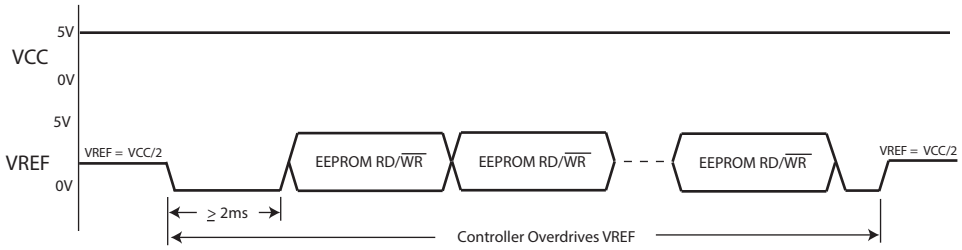

Figure 6: EEPROM Read/$\overline{\text{Write}}$ when ANALOG_LOCK = 0

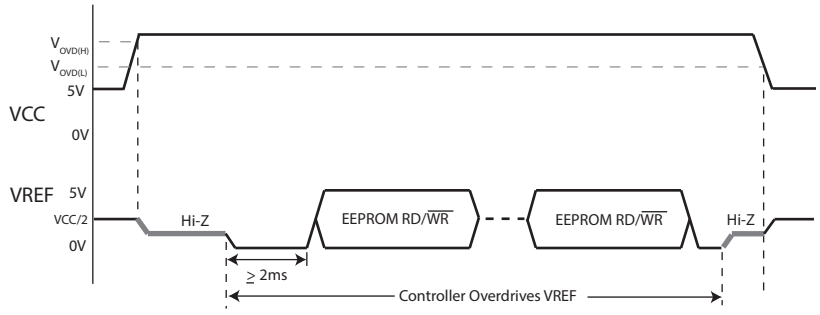

Figure 7: EEPROM Read/$\overline{\text{Write}}$ when ANALOG_LOCK = 1

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Communications Protocol

Write Access Code (Controller to Device)

The fields for the Access Code command are:

- Sync (2 zero bits)
- Read/Write (1 bit)
- Address (6 bits)
- Data (32 bits)
- CRC (3 bits)

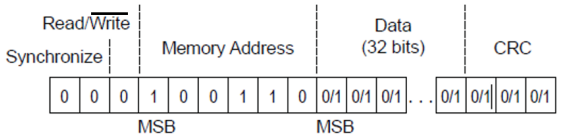

Figure 8: Write Access Code

Read (Controller to Device)

The fields for the Read command are:

- Sync (2 zero bits)
- Read/Write (1 bit)
- Address (6 bits)
- CRC (3 bits)

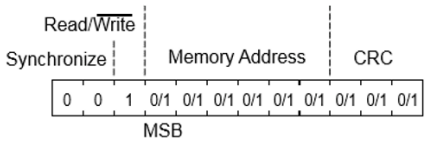

Figure 9: Read Sequence

Read Acknowledge (Device to Controller)

The fields for the data return frame are:

- Sync (2 zero bits)
- Data (32 bits):
  - □ [31:28] Don't Care
  - □ [27:26] ECC Pass/Fail
  - □ [25:0] Data
  - □ CRC (3 bits)

Figure 10 shows the sequence for a Read Acknowledge. Refer to the Detecting ECC Error section for instructions on how to detect memory errors using ECC.

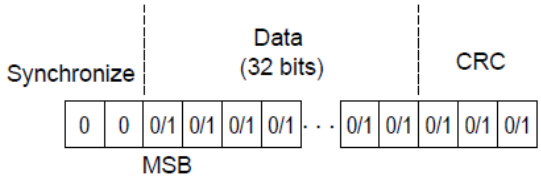

Figure 10: Read Acknowledge Sequence

Write (Controller to Device)

The fields for the Write command are:

- Sync (2 zero bits)
- Read/Write (1 bit)
- Address (6 bits)
- Data (32 bits):
  - □ [31:26] Don't Care
  - □ [25:0] Data
  - □ CRC (3 bits)

Figure 11 shows the sequence for a Write command. Bits [31:26] are Don't Care because the device automatically generates 6 ECC bits based on the content of bits [25:0]. These ECC bits will be stored in EEPROM at locations [31:26].

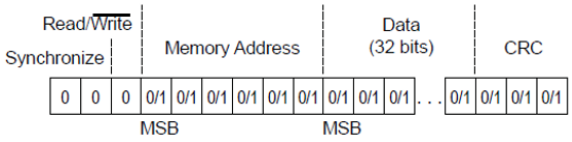

Figure 11: Write Sequence

EEPROM Error Checking and Correction (ECC)

Hamming code methodology is implemented for EEPROM checking and correction. The device has ECC enabled after power-up. The device always returns 32 bits. The message received from controller is analyzed by the device EEPROM driver and ECC bits are added. The first six received bits from device to controller are dedicated to ECC.

Detecting ECC Error

If an uncorrectable error has occurred, bits 27:26 are set to 0x2, the VOUT pin will go to a high-impedance state, and the device will not respond to the applied magnetic field. Table 1 describes the contents of the ECC bit field.

Table 1: ECC Field Descriptions

Bits	Name	Description
31:28	n/a	n/a
27:26	ECC	0x0 – no meaning 0x1 – error detected and corrected 0x2 – uncorrectable error(s) 0x3 – no meaning
25:0	Data	Data bits [25:0]

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ACS37600 Calibration

V_{REF}, offset voltage (QVO), and sensitivity of the ACS37600 are factory-trimmed according to the specifications listed in Table 2. It is recommended that an end-of-line calibration be performed for optimal system accuracy.

Table 2: ACS37600 Factory Settings and Trim Resolution

ACS37600 Version	Specification	Factory Setting	Avg Trim Step Size
1p5B5	Sensitivity	1.5 mV/G	3.7 µV/G
	V_{REF}	2.5 V	1 mV
	Offset Voltage	~0 mV	1 mV
3B5	Sensitivity	3 mV/G	7.5 µV/G
	V_{REF}	2.5 V	1 mV
	Offset Voltage	~0 mV	1 mV
6B5	Sensitivity	6 mV/G	15 µV/G
	V_{REF}	2.5 V	1 mV
	Offset Voltage	~0 mV	1 mV
13B5	Sensitivity	13.5 mV/G	34 µV/G
	V_{REF}	2.5 V	1 mV
	Offset Voltage	~0 mV	1 mV

The recommended order of system trims during calibration is sensitivity followed by QVO. It is expected that the factory-trimmed value for V_{REF} is sufficient so an end of line V_{REF} trim should not be required. There are coarse and fine trims for each parameter; however, only the fine trims should need to be adjusted during calibration. The fine trims for QVO and sensitivity are each controlled by a 9 bit, two's complement trim code: VOFF_FINE and SENS_FINE, respectively. The step size of a 1 LSB adjustment for each of these trims is shown in Table 2. To allow margin for temperature and supply variation, it is recommended that codes used are restricted to 0-223 and 288-511. The transfer function for each of the trimmable parameters is shown in Figure 12.

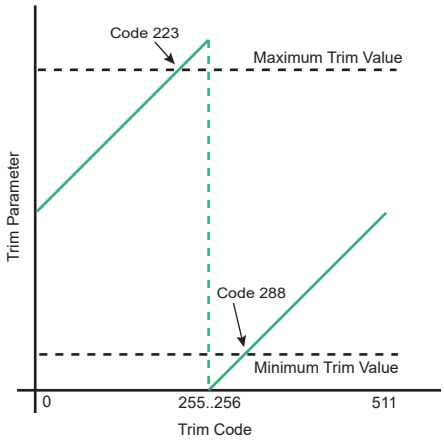

Figure 12: Trim Transfer Function

Sensitivity Trim

Prior to beginning the trims, measure V_{OUT} with zero field applied. Retain this value as V_{QVO}. Once that measurement is made, sensitivity should be trimmed first. It is recommended to trim sensitivity prior to offset because the sensitivity trim may impact the offset. Use the following procedure to trim sensitivity:

1. Read the contents of the SENS_FINE register and apply maximum magnetic field to the device. The maximum magnetic field is determined by the maximum magnetic field that is expected to be seen by the device in the end application. Alternatively, a scaled-down magnetic field can be applied during end-of-line testing and the result can be scaled appropriately.
2. Measure V_{OUT}. This will be V_{MAX}.
3. Compare $V_{MAX} - V_{QVO}$ to the target full scale output voltage swing for maximum magnetic field, V_{FS}. $V_{\Delta SENS} = V_{FS} - (V_{MAX} - V_{QVO})$.
4. Adjust SENS_FINE to trim sensitivity: SENS_FINE = SENS_FINE + $V_{\Delta SENS}/SENS_{STEP}$ where $SENS_{STEP}$ is the sensitivity trim step size.
5. Repeat steps 2-4 until $V_{\Delta SENS} < 0.5 \times SENS_{STEP}$.

Offset Voltage (QVO) Trim

Assuming the desired value of V_{OUT} when no magnetic field is applied is to be equal to V_{REF}, use the following procedure to trim QVO:

1. Read the contents of the VOFF_FINE register.
2. Measure V_{OUT} with no magnetic field applied.
3. Measure V_{REF}.
4. $V_{\Delta QVO} = V_{REF} - V_{OUT}$.
5. Adjust VOFF_FINE to trim the offset voltage: VOFF_FINE = VOFF_FINE + $V_{\Delta QVO}/V_{OFFSTEP}$ where $V_{OFFSTEP}$ is the offset voltage trim step size.
6. Repeat steps 2-4 until $V_{\Delta QVO} < 0.5 \times V_{OFFSTEP}$.

Added Memory Lock Protection

Once calibration is complete, it is strongly recommended that ANALOG_LOCK, (register bit 0x0F[24]), and UNLOCK_CODE, (register bit 0x0F[25]), be set to 1 to lock the memory and ensure against accidental programming in the field.

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Memory Map

Table 3: EEPROM Register Address 0x5

Bits	Name	Type	Default	Description
31:26	ECC_5	R	–	Error correction code
25:24	UNUSED5	R/W	0x0	Not used
23:15	VOFF_FINE	R/W	Factory Trim	Two's complement value for fine tuning of QVO
14:11	SPARE_USER	R/W	0x0	Spare bits with customer access
10	UVD_DIS	R/W	0x0	0x0 - UVD Enabled 0x1 - UVD Disabled
9	OVD_DIS	R/W	0x0	0x0 - OVD Enabled 0x1 - OVD Disabled
8	VOUT_ECO_MODE	R/W	0x0	0x0 - Normal power for VOUT amplifier 0x1 - Activates low power mode for the VOUT amplifier
7:6	IO_REF_MODE	R/W	0x3	VREF pin mode: 0x0 - Input 0x1 - Input 0x2 - Output 0x3 - Input/Output (VREF can be overdriven for programming)
5:4	BE1_BW_SEL	R/W	0x2	Bandwidth selection: 0x0 - 100 kHz 0x1 - 250 kHz 0x2 - 400 kHz 0x3 - Max
3:2	SENS_COARSE	R/W	Device Specific	Coarse sensitivity: 0x0 - 1.3 mV/G 0x1 - 2.6 mV/G 0x2 - 5.2 mV/G 0x3 - 11.7 mV/G
1:0	VREF_COARSE	R/W	0x3	V_{REF} voltage coarse setting: 0x0 - 0.5V 0x1 - 1.5V 0x2 - 1.65V 0x3 - 2.5V

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Table 4: EEPROM Register Address 0x6

Bits	Name	Type	Default	Description
31:26	ECC_6	R	–	Error correction code
25:19	UNUSED6	R/W	0x0	Not used
18	GC_POL	R/W	0x0	Polarity inversion 0x0 - Output increases with positive field perpendicular to top face of package. 0x1 - Output decreases with positive field perpendicular to top face of package.
17:9	OCF_THR	R/W	Factory Trim	Overcurrent fault trim setting. Trimmed at factory for 100% full-scale current.
8	OCF_DIS	R/W	0x0	0x0 - Overcurrent fault enabled 0x1 - Overcurrent fault disabled
7:5	OCF_HOLD	R/W	0x0	OCF hold time: 0x0 - 0 µs, 0x1 - 100 µs, 0x2 - 250 µs, 0x3 - 500 µs, 0x4 - 1.0 ms, 0x5 - 2.0 ms, 0x6 - 3.5 ms, 0x7 - 5.0 ms.
4:2	OCF_MASK	R/W	0x1	OCF masking time: 0x0 - Deglitch filter disabled, 0x1 - Deglitch filter length 0.5 µs, 0x2 - Deglitch filter length 1.0 µs, 0x3 - Deglitch filter length 1.5 µs, 0x4 - Deglitch filter length 2.0 µs, 0x5 - Deglitch filter length 2.5 µs, 0x6 - Deglitch filter length 3.0 µs, 0x7 - Deglitch filter length 3.5 µs.
1	OCF_PERSIST	R/W	0x0	0x0 - OCF clears when OCF condition no longer exists and hysteresis has been satisfied. 0x1 - OCF can only be cleared with a power cycle.
0	OCF_HYS	R/W	0x0	0x0 - Standard hysteresis 0x1 - Doubles the hysteresis

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Table 5: EEPROM Register Address 0xF

Bits	Name	Type	Default	Description
31:26	ECC_F	R	–	Error correction code
25	UNLOCK_CODE	R/W	0x0	0x0 - No unlock code required prior to the access code when initiating communications. 0x1 - Communications to the device requires an unlock code prior to the access code when initiating communications.
24	ANALOG_LOCK	R/W	0x0	0x0 - No OVD condition on VCC required to communicate with device. VREF must be overdriven for communications. 0x1 - Requires OVD condition on VCC in order to enable communications on VREF. When an OVD condition is sensed by the device, VREF will be put into a high-impedance state enabling ease of overdriving.
23:18	GAIN_TC	R/W	0x0	Two's complement, linear sensitivity adjustment for system temperature compensation. Step size = 0.0026%/°C
17:9	SENS_FINE	R/W	Factory Trim	Two's complement value for fine tuning of sensitivity.
8:0	VREF_FINE	R/W	Factory Trim	Two's complement value for fine tuning of VREF.

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Revision History

Number	Date	Description
–	July 8, 2020	Initial release

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