Product Information

Allegro Package Designations

INTRODUCTION

This document provides reference information as an aid to differentiating the device package types used by Allegro™ MicroSystems. It provides cross-references to the *package designation*, an Allegro code that is integrated into the device part number:

- alphabetical listing of Allegro package designators, with differentiating specifications and reference illustrations
- alphabetical listing of common or obsolete package designators, cross-referenced to Allegro designators
- key to interpreting Allegro part numbers for package designators
- key to interpreting Allegro terms for lead forms

The package designator is used to differentiate the external physical characteristics of the packages for ordering purposes.

To use this document, in the Allegro Package Code column, locate the package designator for the device. Alternatively, use the drawings to identify a package, or the cross-reference to common terms.

A few package types have leadform options. These options are indicted by the *instruction* codes, shown in parentheses in the Package Designation column. Leadform options are shown in separate rows. Leadform options are not always available for every device type.

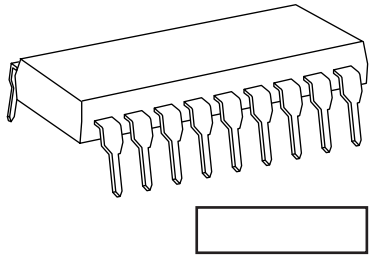
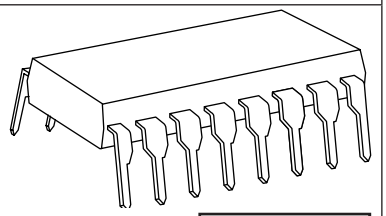
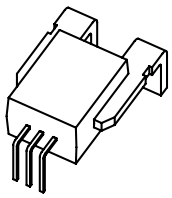
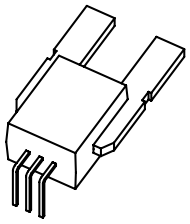
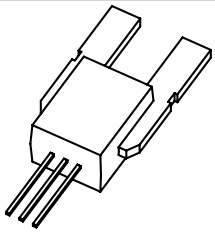
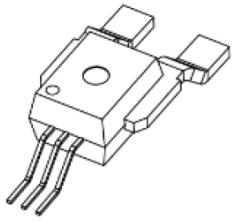
The options available for any specific device are substantially determined by the package designation for that device. Not all options are available for any particular package designation or device type, and provision of certain configurations may be subject to minimum volume or NCNR (noncancellation, non-return) limitations.

For clarity and differentiation, the drawings are schematic and not to scale, however, a representative footprint is provided at approximately actual size of the package body when mounted on a PCB. The drawings do not represent all possible configurations of that device, or any particular device, and may have features that vary according to supplier preference within specifications, such as pin 1 index marks. Exposed thermal pads may have several alternative layouts for any particular package designation.

When applicable, references to industry-standard type conventions, such as JEDEC package registrations, are provided. These references are for informational purposes only, and do not necessarily indicate that the device indicated conforms fully with those standards in all respects.

NOTE: For information on packages and leadform configurations offered for individual devices, refer to the datasheet for the device.

PACKAGE DESIGNATORS

Package Designator	Package Type (Common Package Designator)	JEDEC Package Outline	Quantity of Terminals	Pictorial View/ Representative Footprint
A	Plastic dual in-line (DIP/PDIP/DIL/PDIL); Through-hole pin, 300 mil row spacing; "BB" half-lead end pins. OBSOLETE	MS-001AA MS-001AC MS-001AD MS-001AF	14 18 20 24	
	Plastic dual in-line (DIP/PDIP/DIL/PDIL); Through-hole pin, 300 mil row spacing (width measured at shoulders of leads); End pins are half-leads	–	16	
	Plastic dual in-line (DIP/PDIP/DIL/PDIL); Through-hole pin, 400 mil row spacing; OBSOLETE	MS-010AA	22	
	Plastic dual in-line (DIP/PDIP/DIL/PDIL); Through-hole pin, 600 mil row spacing; OBSOLETE	MS-011AB	28	
B	Semi-tab plastic dual in-line (DIP/PDIP/DIL/PDIL) with internally fused leads, both sides; Through-hole pin, 300 mil row spacing; "BB" half-lead end pins; OBSOLETE	MS-001BB MS-001AF	16 24	
CB-PFF	Plastic case with internally fused primary conductor leads for sensed current; Through-hole pin	–	5	
CB-PSF	Plastic case with internally fused primary conductor leads for sensed current; Through-hole/weld pin	–	5	
CB-PSS	Plastic case with internally fused primary conductor leads for sensed current; Through-hole/weld pin	–	5	
CB-SMT	Plastic case with internally fused primary conductor leads for sensed current; Through-hole/weld pin	–	5	

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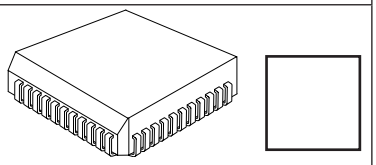
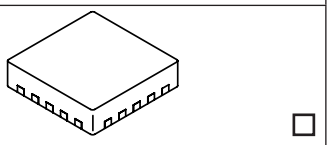
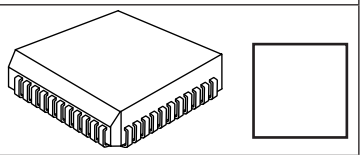
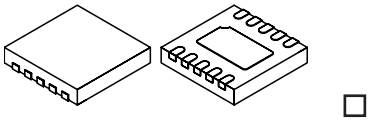
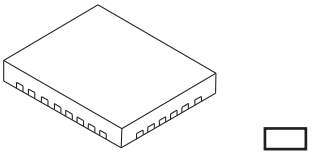
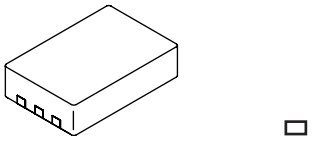
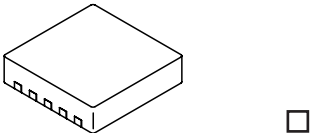
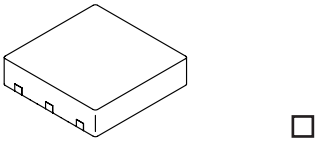
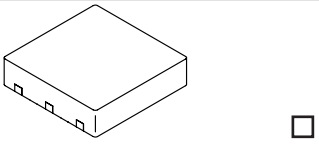
Package Designator	Package Type (Common Package Designator)	JEDEC Package Outline	Quantity of Terminals	Pictorial View/ Representative Footprint
CG	Bare die with solder bumps (WLCSP)	–	Various	
CW	Wafer with bare die	–	Various	–
EB	Plastic leaded chip carrier (PLCC/PQCC); square body; internally fused leads, two opposite sides; Socket J lead; OBSOLETE	MS-018AB MS-018AC	28 44	
EC	Plastic leadless package with quad (4) populated sides and exposed thermal pad (MLPQ/QFN); square body, 0.75 mm nominal (0.80 maximum) height; Surface-mount contacts, 0.40 mm contact pitch	MO-220WGGE	26	
ED	Plastic leaded chip carrier (PLCC/PQCC); square body; internally fused leads, four sides; Socket J lead; OBSOLETE	MS-018AC	44	
EE	Plastic leadless package with dual (2 opposite) populated sides and exposed thermal pad (MLPD/DFN/SON); square body, variable footprint; 0.60 mm maximum height (ultra-thin profile) Surface-mount contacts, 0.50 mm contact pitch	MO-229UCCD	8, 10	
EG	Plastic leadless package with quad (4) populated sides and exposed thermal pad (QFN); rectangular body, 4 × 5 mm, 0.75 mm nominal (0.80 maximum) height; Surface-mount contacts, 0.50 mm contact pitch	MO-229WDED	28	
EH	Plastic leadless package with dual (2 opposite) populated sides (shorter sides) and exposed thermal pad (MLPD/DFN/SON); rectangular body, 2 × 3 mm, 0.75 mm nominal (0.80 maximum) height; Surface-mount contacts, 0.50 mm contact pitch	MO-229WCED Type1	6	
EJ	Plastic leadless package with dual (2 opposite) populated sides and exposed thermal pad (MLPD/DFN/SON); square body, 3 × 3 mm footprint; 0.75 mm nominal (0.80 maximum) height; Surface-mount contacts, 0.50 mm contact pitch	MO-229WEED	10	
EK	Plastic leadless package with dual (2 opposite) populated sides and exposed thermal pad (MLPD/DFN/SON); square body, variable footprint; 0.75 mm nominal (0.80 maximum) height; Surface-mount contacts, 0.95 mm contact pitch	MO-229WEEA	5, 6 (OBS)	
EL	Plastic leadless package with dual (2 opposite) populated sides and exposed thermal pad (MLPD/DFN/SON); square body, variable footprint, 0.55 mm maximum height (ultra-thin profile); Surface-mount contacts, 0.50 mm contact pitch; OBSOLETE	MO-229UCCD	3, 6	

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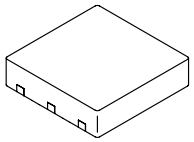
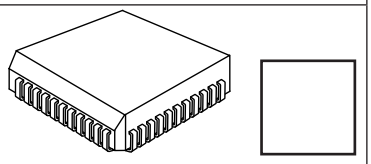
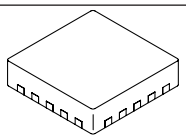
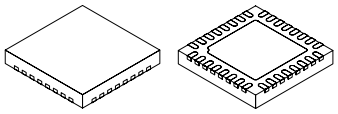
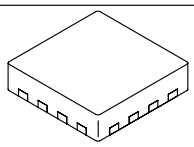
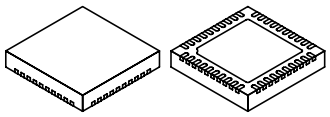
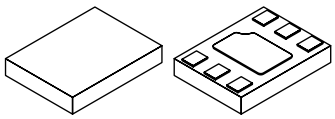
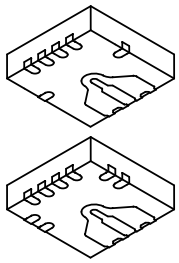
Package Designator	Package Type (Common Package Designator)	JEDEC Package Outline	Quantity of Terminals	Pictorial View/ Representative Footprint
EM	Plastic leadless package with dual (2 opposite) populated sides and exposed thermal pad (MLPD/DFN/SON); square body, variable footprint, 0.45 mm nominal (0.50 mm maximum) height; Surface-mount contacts, 0.65 mm contact pitch; OBSOLETE	MO-229XCCC	5	
EP	Plastic leaded chip carrier (PLCC/PQCC); square body; Socket J lead; OBSOLETE	MS-018AA MS-018AB MS-018AC	20 28 44	
ES	Plastic leadless package with quad (4) populated sides and exposed thermal pad (MLPQ/QFN); square body, 0.75 mm nominal (0.80 maximum) height; Surface-mount contacts, 0.50 mm contact pitch	MO-220WEED MO-220WGGD	12, 16 20, 24	
ET	Plastic leadless package with quad (4) populated sides and exposed thermal pad (MLPQ/QFN); square body, 5 × 5 mm maximum footprint; 0.90 mm nominal height (1.00 maximum); Surface-mount contacts, 0.50 mm contact pitch	MO-220VHHD	28, 32	
EU	Plastic leadless package with quad (4) populated sides and exposed thermal pad (MLPQ/QFN); square body, 4 × 4 mm footprint, 0.75 mm nominal (0.80 mm maximum) height; Surface-mount contacts, 0.65 mm contact pitch	MO-220WGGC	16	
EV	Plastic leadless package with quad (4) populated sides and exposed thermal pad (MLPQ/QFN); square body, variable footprint; 0.90 mm nominal (1.00 maximum) height; Surface-mount contacts, 0.50 mm contact pitch	MO-220VJJD MO-220VKKD	36, 40 48	
EW	Plastic leadless package with dual (2) populated sides and exposed thermal pad (MLPD/DFN/SON); rectangular body, 0.40 mm maximum height (super-thin profile) Surface-mount contacts, variable footprint (including pullback contacts), 0.50 mm contact pitch	MO-229X2BCD Type1	6	
EX	Plastic leadless package with quad (4) populated sides and exposed current loop (MLPQ/QFN); square body, 3 × 3 mm footprint; 0.75 mm nominal height (0.80 maximum); Surface-mount contacts, 0.50 mm contact pitch	MO-220WEED	10 12	

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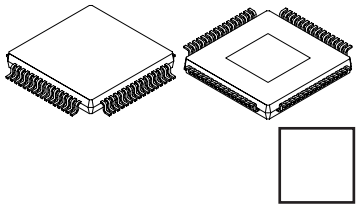
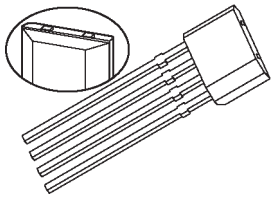
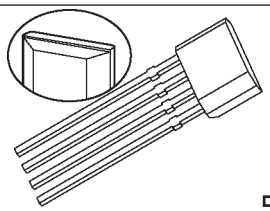
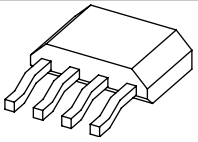
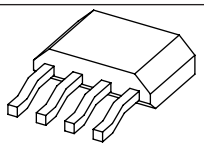
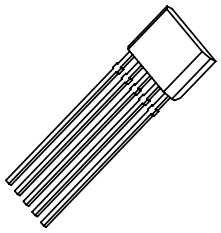
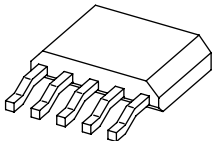
Package Designator	Package Type (Common Package Designator)	JEDEC Package Outline	Quantity of Terminals	Pictorial View/ Representative Footprint
JP	Plastic low-profile quad flatpack with exposed thermal pad (LQFP, eLQFP); 1.4 mm nominal body thickness; Gull-wing surface-mount	MS-026BBCHD	32, 48	
JS	Plastic thin-profile quad flatpack with exposed thermal pad (TQFP, eTQFP); 1.0 mm nominal body thickness; Gull-wing surface-mount, 0.50 mm contact pitch	MS-026ADDHD	80	
JU	Plastic thin-profile quad flatpack (TQFP); 1.0 mm nominal body thickness; Gull-wing surface-mount, 0.50 mm contact pitch; OBSOLETE	MS-026ABC	48	
K (none)	Plastic single in-line (SIP), matrix; Through-hole pin; Flat tie bar burr area at case top	–	4	
	Plastic single in-line (SIP), conventional; Through-hole pin; no tie bars at case top OBSOLETE	–	4	
K (TL,TS)	Plastic single in-line (SIP); Pins formed for horizontal body mounting	–	4	
K (TW)	Plastic single in-line (SIP); Pins formed for horizontal body mounting	–	4	
KA (none)	Plastic single in-line (SIP); Through-hole pin	–	5	
KA (TL,TS)	Plastic single in-line (SIP); Pins formed for horizontal body mounting	–	5	

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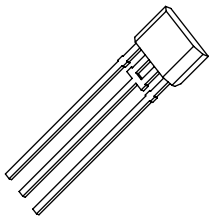
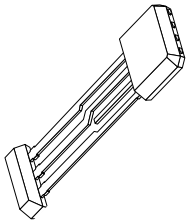
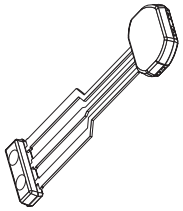
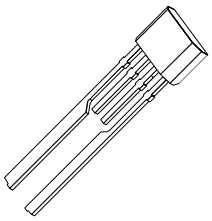
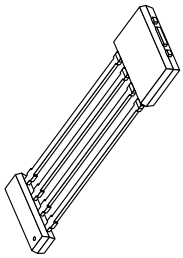
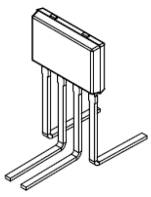
KB	Plastic single in-line (SIP); Through-hole pin	–	3	
KC	Plastic single in-line (SIP); Through-hole pin	–	3	See KB
KE	Plastic single in-line (SIP); Through-hole pin	–	4	
KH	Plastic single in-line (SIP); Through-hole pin	–	3	
KN	Plastic single in-line (SIP); Through-hole pin	–	4	
KT	Plastic single in-line (SIP); Through-hole pin	–	4	
KT (TF)	Plastic single in-line (SIP); Through-hole pin	–	4	

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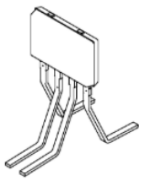
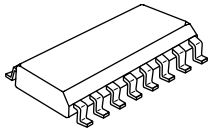
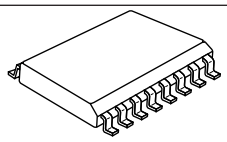
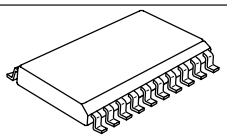
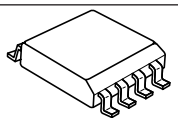
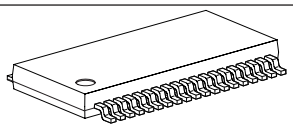
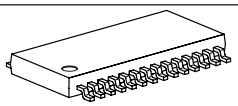
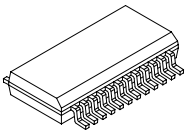
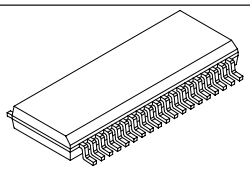
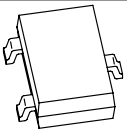
Package Designator	Package Type (Common Package Designator)	JEDEC Package Outline	Quantity of Terminals	Pictorial View/ Representative Footprint
KT (TH)	Plastic single in-line (SIP); Through-hole pin	–	4	
L	Plastic small-outline IC (SOIC, SO, SOP); 3.90 mm/150 mil body width; Gull-wing surface-mount, 1.27 mm lead pitch	MS-012AA MS-012AB MS-012AC	8 (NND), 14 (OBS), 16 (OBS)	
LA	Plastic small-outline IC (SOIC-W, SOP) with internally fused primary conductor leads for sensed current; 7.50 mm/300 mil body width; Gull-wing surface-mount, 1.27 mm lead pitch	MS-013AA	16	
LB	Plastic small-outline IC (SOIC-W, SOP) with internally fused leads or external semitab, both sides; 7.50 mm/300 mil body width; Gull-wing surface-mount, 1.27 mm lead pitch	MS-013AA MS-013AC MS-013AD MS-013AE	16, 20 (OBS), 24, 28 (OBS)	
LC	Plastic small-outline IC (SOIC, SO, SOP) with internally fused primary conductor leads for sensed current; 3.90 mm/150 mil body width; Gull-wing surface-mount, 1.27 mm lead pitch	MS-012AA	8	
LD	Plastic thin-shrink small-outline IC (TSSOP); 4.4 mm body width; Gull-wing surface-mount, 0.50 mm lead pitch	MO-153BD-1	38	
LE	Plastic thin-shrink small-outline IC (TSSOP); 4.4 mm body width; Gull-wing surface-mount, 0.65 mm lead pitch	MO-153AC	8, 14, 20, 24	
LF	Plastic small-outline IC (QSOP, appearance like SOIC) sensor variant with internally fused primary conductor leads for sensed current; 3.90 mm body width; Gull-wing surface-mount, 0.635 mm lead pitch	MO-137AE	24	
LG	Plastic thin-shrink small-outline IC (TSSOP); with internally fused leads, both sides; 4.4 mm body width; Gull-wing surface-mount, 0.50 mm lead pitch	MO-153BD-1	38	
LH	Plastic small-outline transistor (SOT23W-3, SOHED); 1.98 mm body width; Mini gull-wing surface-mount	–	3, 5	

PUB26013, Rev. 8
MCO-0000225

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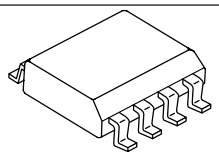
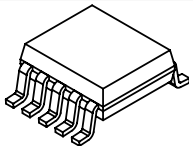
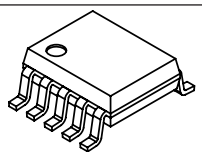
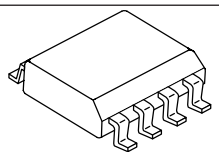
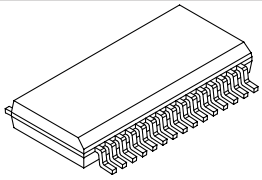
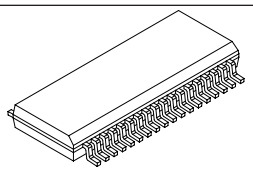
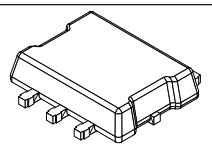
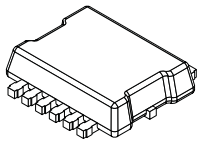
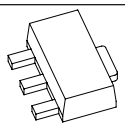
Package Designator	Package Type (Common Package Designator)	JEDEC Package Outline	Quantity of Terminals	Pictorial View/ Representative Footprint
LJ	Plastic small-outline IC (SOIC, SO, SOP) with exposed thermal pad; 3.90 mm/150 mil body width; Gull-wing surface-mount, 1.27 mm lead pitch	MS-012BA	8	
LK	Plastic small-outline IC (SOIC) with exposed thermal pad; 3.90 mm/150 mil body width; Gull-wing surface-mount, 1 mm lead pitch	–	10	
LL	Plastic small-outline transistor, thermally enhanced with exposed ground tab (SOT89, SC-62); Surface-mount flat lug lead	TO-243AA	3	
LN	Plastic small-outline IC (SOIC, SSOP); 3.90 mm/150 mil body width; Gull-wing surface-mount, 1.00 mm lead pitch	–	10	
LO	Plastic small-outline IC (SOIC, SO, SOP); 3.90 mm/150 mil body width; Gull-wing surface-mount, 1.27 mm lead pitch; NND	MS-012AA	8	
LP	Plastic thin-shrink small-outline IC with exposed thermal pad (TSSOP); Gull-wing surface-mount, 0.65 mm lead pitch; 4.4 mm body width	MO-153ABT MO-153ACT MO-153ADT MO-153AET	16 20 24 28	
LQ	Plastic small-outline IC (QSOP, appearance like SOIC); 7.50 mm/300mil body width; Gull-wing surface-mount, 0.80 mm lead pitch	–	36, 44	
LR	Plastic small-outline flip-chip design IC (PSOF); 1.6 mm pitch primary leads with exposed current loop	–	7	
LS	Plastic small-outline flip-chip design IC (PSOF); 0.8 mm pitch primary leads with exposed current loop	–	10	
LT	Plastic small-outline transistor, thermally enhanced with exposed ground tab (SOT89, SC-62); Surface-mount flat lug lead	TO-243AA	3	

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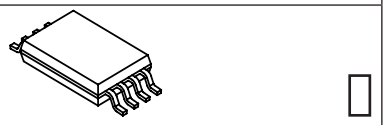
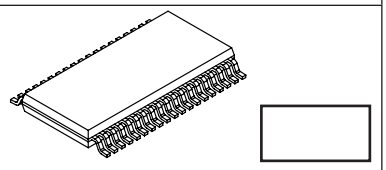
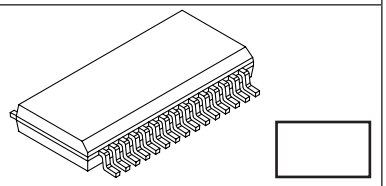
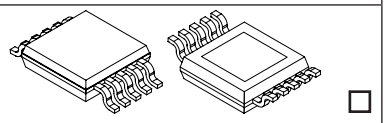
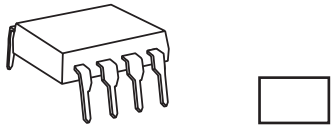
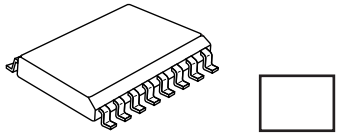
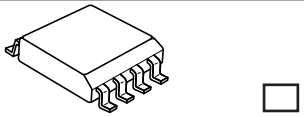
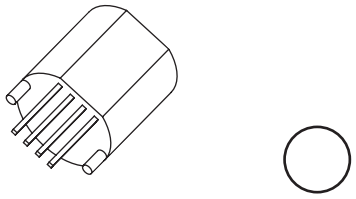
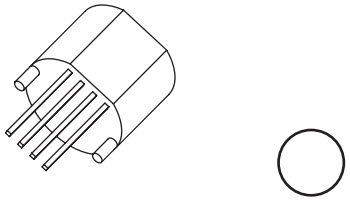
Package Designator	Package Type (Common Package Designator)	JEDEC Package Outline	Quantity of Terminals	Pictorial View/ Representative Footprint
LU	Plastic thin-shrink small-outline IC (TSSOP) 4.4 mm body width; Gull-wing surface-mount, 0.65 mm lead pitch	–	8, 14	
LV	Plastic thin-shrink small-outline IC (TSSOP) with exposed thermal pad; 4.4 mm body width; Gull-wing surface-mount, 0.50 mm lead pitch	MO-153BDT	38	
LW	Plastic small-outline IC (SOIC-W, SOP); 7.50 mm/300 mil body width; Gull-wing surface-mount, 1.27 mm lead pitch	MS-013AA MS-013AB MS-013AC MS-013AD MS-013AE	16, 18 (OBS), 20, 24, 28 (OBS)	
LY	Mini small-outline (MSOP, SOP: appearance like TSSOP) with exposed thermal pad; Gull-wing surface-mount, 0.50 mm lead pitch	MO-187BA-T	10	
M	Mini plastic dual in-line (DIP/PDIP); 300 mil row spacing, half-lead end pins; Through-hole pin; OBSOLETE	MS-001BA	8	
MA	Plastic small-outline IC (SOIC-W); 7.50 mm/300 mil body width; Gull-wing surface-mount, 1.27 mm lead pitch	MS-013AA	16	
OL	Plastic small-outline IC (SOIC); 3.90 mm/150 mil body width; Gull-wing surface-mount, 1.27 mm lead pitch	–	8	
SA	Plastic case (SIP); 9 mm body height; Through-hole pin OBSOLETE	–	4	
SB	Plastic case (SIP); 7 mm body height; Through-hole pin NND	–	4	

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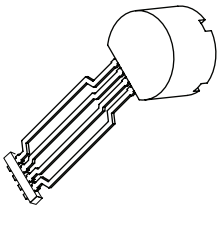
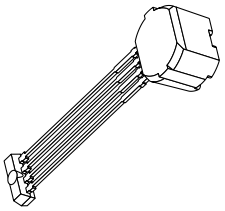
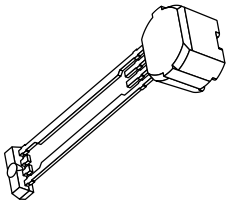
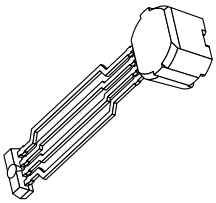
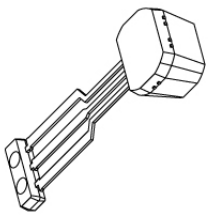
SE	Plastic single in-line (SIP), round top; Spread pins; Through-hole pin; Molded lead bar	–	4	
SG	Plastic single in-line (SIP), flat top; Straight full pins; Through-hole pin; Molded lead bar	–	4	
SH	Plastic single in-line (SIP), flat top; Pins 2 and 3 clipped, pins 1 and 4 wide; Through-hole pin; Molded lead bar	–	4	
SJ	Plastic single in-line (SIP), flat top; Spread pins; Through-hole pin; Molded lead bar	–	4	
SL	Plastic single in-line (SIP); 9.65 mm diameter, 6.00 mm thick case, OR 10.0 mm diameter, 6.00 mm thick case; Spread pins; Through-hole pin; Molded lead bar	–	3	
SM	Plastic single in-line (SIP); 8.0 mm diameter, 5.00 mm thick case; Spread pins; Through-hole pin; Molded lead bar	–	3	

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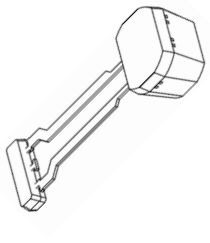
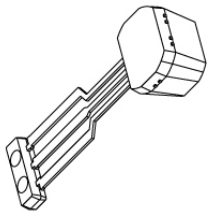
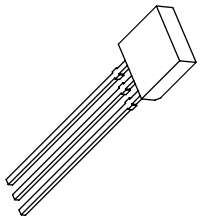
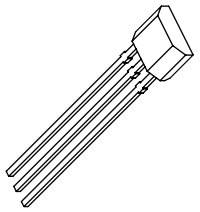
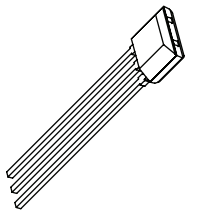
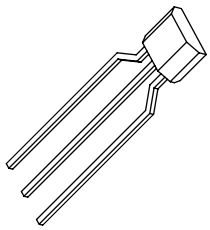
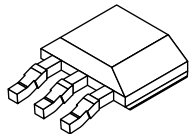
SN	Plastic single in-line (SIP); 8.0 mm diameter, 5.00 mm thick case; Spread pins; Through-hole pin; Molded lead bar	–	3	
SP	Plastic single in-line (SIP); 8.0 mm diameter, 5.00 mm thick case; Spread pins; Through-hole pin; Molded lead bar	–	3	
U	Plastic mini single in-line (SIP); Through-hole pin OBSOLETE	–	3	
UA (TI,TN, TJ)	Conventional. Plastic ultra-mini single in-line (SIP); Through-hole pin, 1.27 mm pin pitch, 15.75 mm leads	–	3	
	Matrix. Plastic ultramini single in-line (SIP); Through-hole pin, 1.27 mm pin pitch, 14.99 mm leads	–	3	
UA (LC,TA)	Plastic ultra-mini single in-line (SIP); Through-hole pin, 2.54 mm pin pitch, conventional or matrix	–	3	
UA (TL,TS)	Plastic ultra-mini single in-line (SIP); Pins formed for horizontal body mounting; 50 mil pin pitch, conventional or matrix	–	3	

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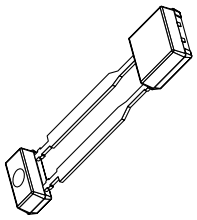
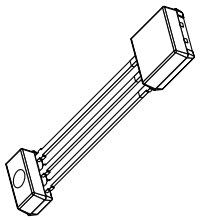
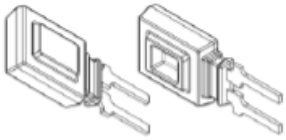
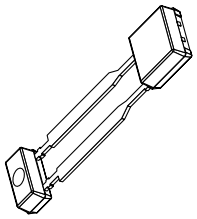
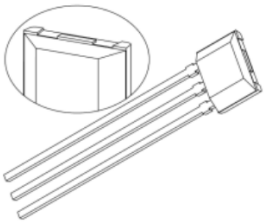
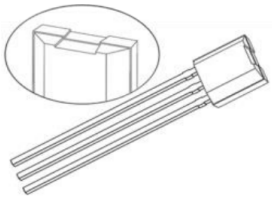
Package Designator	Package Type (Common Package Designator)	JEDEC Package Outline	Quantity of Terminals	Pictorial View/ Representative Footprint
UB	Plastic mini single in-line (SIP); Through-hole pin; Molded lead bar	–	2	
UC	Plastic mini single in-line (SIP); Through-hole pin; Molded lead bar	–	3	
UD	Plastic mini single in-line (SIP); Through-hole pin	–	2	
UE	Plastic mini single in-line (SIP); Through-hole pin; Molded lead bar	–	2	
UF	Plastic ultramini single in-line (SIP); Through-hole pin. Variant of UA – gate relief package, without tiebars	–	3	
UG	Plastic ultramini single in-line (SIP); Through-hole pin. Sensors Hall device with straight leads. 4.06 mm × 4.05 mm package body with no lead bar.	–	3	

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COMMON PACKAGE TERM CROSS-REFERENCE

Common Configuration Terms

Term	Package Designator
CSP	CG
DFN	EE EF EH EJ EK EL EM EW
DIP	A B M
LQFP	JP
MSOP	LY, LZ
PLCC	EA EB ED EP EQ
PSOF	LR LS
QFN	EG ES ET EU EV EX
QSOP	LF LQ

Term	Package Designator
SIP	K KA KB KH KT SA SB SE SG SH SJ SL SM SN U UA UB UC UD UF UG
SOIC-N	L LC LJ LK LN LO
SOIC-W	LA LB LW MA
SOT23	LR
SOT23-W	LH
SOT89	LL LT
TQFP	JS JU
TSSOP	LD LE LG LP LU LV
Wafer (undiced)	CW
WLCSP	CG

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COMMON PACKAGE TERM CROSS-REFERENCE (continued)

Alternative Terms for Configurations (other industry terms or obsolete)

Term	Package Designator
Bumped Die	CG
DIL	See DIP
eTSSOP	See LP
Flip Chip	CG
G2000	SE SG SH SJ
HED	K KA KB KC KT U UA UB UC UD UE UF UG

Term	Package Designator
HTSSOP	See LP
MLP	See DFN and QFN
MLPD	See DFN
MLPQ	See QFN
PDIL	See DIP
PDIP	See DIP
PQCC	See PLCC
PQFN	See QFN
PSON	See DFN
SC-62	LT
SO	L LC LJ
SOHED	LH
SOIC appearance	See QSOP

Term	Package Designator
SOP	L LA LB LC LJ LW LZ
SON	See DFN
TDFN	See DFN
TSSOP appearance	See MSOP

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MCO-0000225

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QFN/DFN/SON/MLP DIMENSIONAL CROSS-REFERENCE

Sort by Contact Pitch			
	Pitch (mm)	Maximum Height (mm)	Size Constraint
EC	0.40	0.80	
EE	0.50	0.60	
EG	0.50	0.80	4 mm × 5 mm max
EH	0.50	0.80	Type 1
EJ	0.50	0.80	
EL	0.50	0.55	
ES	0.50	0.80	
ET	0.50	1.00	5 mm × 5 mm max
EV	0.50	1.00	6 mm × 6 mm min
EW	0.50	0.40	Type 1
EX	0.50	0.80	
EM	0.65	0.50	
EU	0.65	0.80	
EK	0.95	0.80	
EF	1.27	1.00	Type 2

Sort by Overall Package Height			
	Maximum Height (mm)	Pitch (mm)	Size Constraint
EW	0.40	0.50	Type 1
EM	0.50	0.65	
EL	0.55	0.50	
EE	0.60	0.50	
EC	0.80	0.40	
EH	0.80	0.50	Type 1
EJ	0.80	0.50	
EK	0.80	0.95	
ES	0.80	0.50	
EU	0.80	0.65	
EX	0.80	0.50	
EF	1.00	1.27	Type 2
ET	1.00	0.50	5 mm × 5 mm max
EV	1.00	0.50	6 mm × 6 mm min

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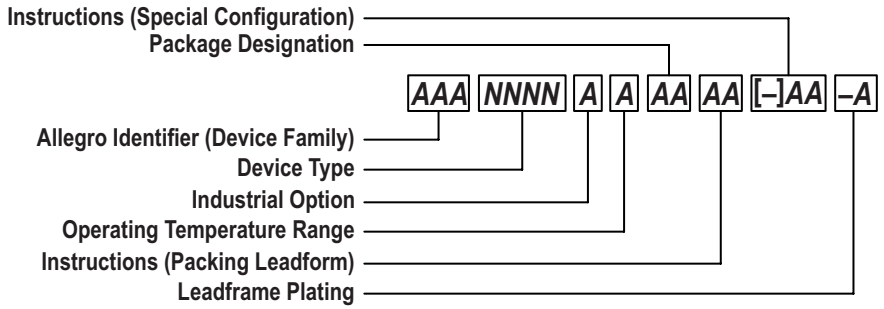
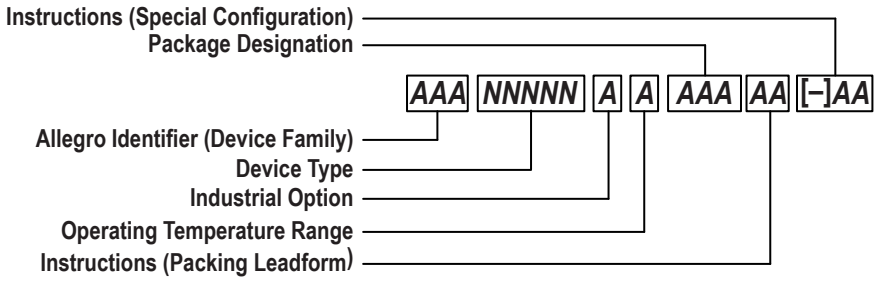
Complete Part Numbers

Complete Part Number Format
("A" initial character style, general product lines)



Allegro Identifier	[*A,* and optional 1 to 2 letters]
Device Type	[3 to 4 numbers] functional type
Industrial Option	[optional 1 letter] blank indicates default configuration; N: industrial
Operating Temperature Range	[1 letter] ambient temperature range
Package Designation	[1 or 2 letters] body configuration
Instructions (Finishing)	Leadform/packing option, etc. Blank indicates default configuration
Leadframe Plating	["-" and 1 letter] nonlead (Pb-free) option

Complete Part Number Format
("A" initial character style, for all part numbers with 5-digit device type)



Allegro Identifier	[*A,* and optional 1 to 2 letters]
Device Type	[5 numbers] functional type
Industrial Option	[optional 1 letter] blank indicates default configuration; N: industrial
Operating Temperature Range	[1 letter] ambient temperature range
Package Designation	[3 letters] body configuration
Instructions (Finishing)	Leadform/packing option, etc. Blank indicates default configuration

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MCO-0000225

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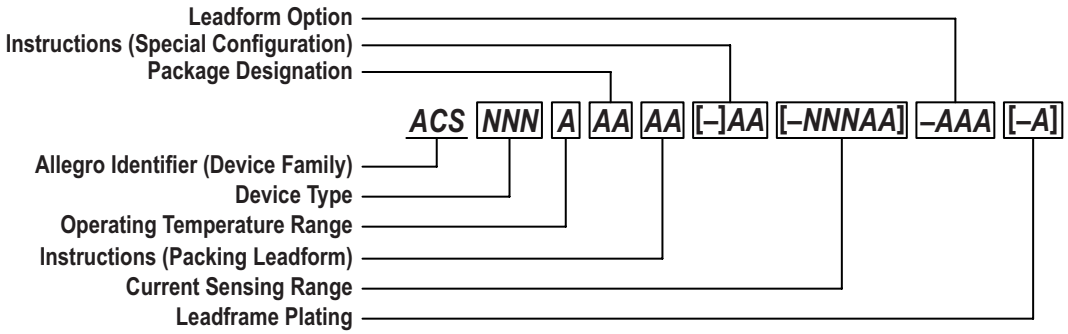
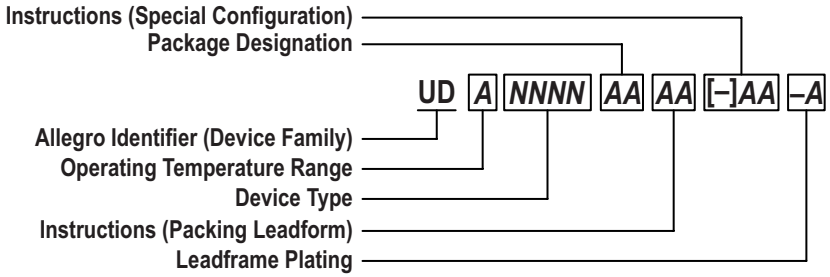
Complete Part Numbers (continued)

Complete Part Number Format
(Sensed current range style, current sensor IC product lines)



Allegro Identifier	ACS
Device Type	[3 numbers] functional type
Operating Temperature Range	[1 letter] ambient temperature range
Package Designation	[1 or 2 letters] body configuration
Instructions (Finishing)	Leadform/packing option, etc. Blank indicates default configuration
Current Sensing Range	[3 numbers] optimal sensing amperage range
	[1 letter] measurable sensing range multiplier. A: 1 × optimal, B: 2 × optimal, C: 3 × optimal
	[1 letter] current direction measurable. B: bidirectional, U: unidirectional
Leadform (75x series)	[3 letters] PFF: formed signal leads, formed current terminals, PSF: formed signal leads, straight current terminals, PSS: straight signal leads, straight current terminals
Leadframe Plating	["-" and 1 letter] nonlead (Pb-free) option

Complete Part Number Format
("U" initial character style, general product lines)



Allegro Identifier	UD
Operating Temperature Range	[1 letter] ambient temperature range
Device Type	[3 to 4 numbers] functional type
Package Designation	[1 or 2 letters] body configuration
Instructions (Finishing)	Leadform/packing option, etc. Blank indicates default configuration
Leadframe Plating	["-" and 1 letter] nonlead (Pb-free) option

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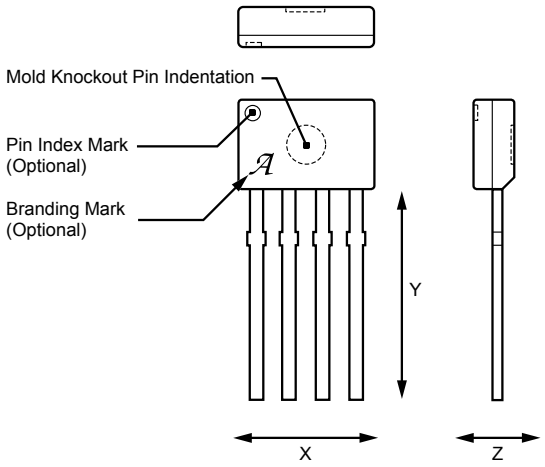
Terms Used to Describe Lead Configurations

Term	Description	Example
X Direction Separation		
Straight	Straight over full length, and perpendicular to package surface	K
Spread	Straight at package surface, with increased pitch after bend	SJ
Fused leads	Internally fused leads for increased thermal conductance (formerly: *semi-tab*)	LB
Joined	Straight at package surface, with merge after bend	KB
Y Direction Length		
Untrimmed	All leads at longer length	UA (TI ordering Instruction)
Trimmed	All leads at shorter length	UA (TL ordering Instruction)
Clipped	Some leads shorter than other leads	SH
Z Direction Offset		
Flat	Straight and perpendicular to package surface	UA (TI ordering Instruction)
Offset	Bent toward mounting surface, then parallel to mounting surface	UA (TL ordering Instruction)



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Revision History

Number	Date	Description
4	July 31, 2017	Added LR, LS, LU, K matrix, SM, SN, and UC packages
5	July 10, 2018	Added EX-10, KH-3, LO-8, SP-3, and UE-3 packages; corrected LU package
6	September 19, 2019	Updated ED, EL, LO, SB package status; corrected JP, JS references; added KT (TF) package leadform; added SL package; other minor editorial updates
7	July 27, 2021	Added CB-SMT, LL, and UD packages; added LU 14 lead count package; corrected SN package lead count
8	August 18, 2021	Updated B package status from NND to OBSOLETE; added KT (TH) package leadform, UF and UG packages; added industrial-grade option to part numbering guide

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