Logic I/O Voltage Configuration Guide for Demonstration Board for AMT49107

ABSTRACT

This guide applies to the Allegro APEK49107 demonstration board, which is designed for Allegro AMT49107 devices. This guide describes how to change the input/output (I/O) voltage logic level of the AMT49107 device fitted to the APEK49107.

INTRODUCTION

APEK49107 (identification number EDC174 on solder-side silk screen) is a demonstration board that carries a soldered-down AMT49107KEVSR-3-T gate driver IC. This part variant is configured by default for operation in conjunction with 3.3 V CMOS logic systems, as are the related features on the board. To operate the board in conjunction with 5 V CMOS logic systems, both the device and board should be reconfigured. A procedure to do this is described in this document along with another that describes how to reverse the change.

Note that orders can be placed for sample and production quantities of AMT49107 parts configured by default for 3.3 V or 5 V logic operation (part numbers AMT49107KEVSR-3-T and AMT49107KEVSR-5-T, respectively). Further information on this can be found in the AMT49107 product datasheet.

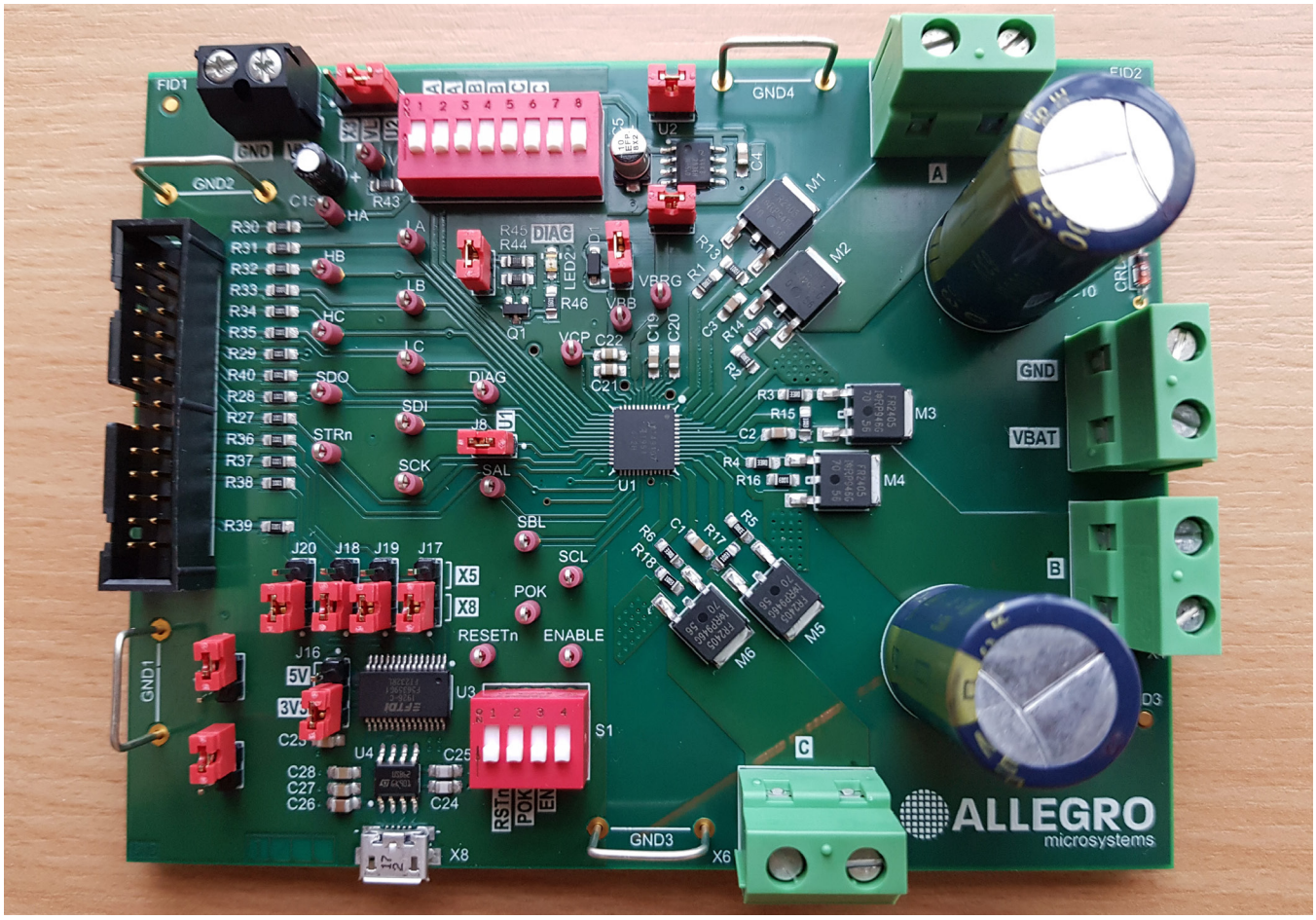

Figure 1: APEK49107 Demonstration Board Photograph

OVERVIEW

Demonstration Board

The APEK49107 demonstration board—shown in the photograph in Figure 1 and in the schematics in Appendix 1—includes:

- AMT49107KEVSR-3-T gate driver IC (U1), default logic input/output levels configured for 3.3 V operation.
- FT232RL USB UART IC (U3):
  - □ A standard USB-A to USB-Micro-B cable plugged into connector X8 is used to connect the USB UART IC to a PC running the Allegro AMT49107 graphical user interface (GUI).
- DC power connector (X2):
  - □ DC power must comply with the non-volatile memory (NVM) programming voltage limit and the VBB functional operating range for the device, as specified in the product datasheet in effect—between 24 V(minimum) and 50 V(maximum), current limit ≥ 50 mA.
  - □ DC power is connected to the board via connector X2.
  - □ The VBAT pin (X2.1) is positive with respect to the GND (X2.2) pin.
- On-board linear regulator (U2):
  - □ The regulator provides a DC bias voltage to allow the AMT49107 discrete control input steady states to be optionally set by way of DIP switches S1 and S2.

Logic I/O Level Control

Logic I/O level control must be set for both the AMT49107 gate driver IC and the FT232RL USB UART IC. However, damage will not result if an incompatibility exists between the I/O voltage settings (i.e., if one device is set for 3V3 operation and the other is set for 5 V operation).

Controls are as follows:

- AMT49107 gate driver IC (U1)
  Logic I/O voltage supply and associated logic thresholds are set by the value of the VIO Voltage Monitor (VLM) bit in the Config 6 register of the device:
  - □ VLM = 0 sets the device to operate with 3.3 V logic.
  - □ VLM = 1 sets the device to operate with 5 V logic.

  To set the VLM bit, the desired value must be written to the Config 6 register over the serial interface. To retain a new VLM bit value between power-up events, the new value must be saved to the internal device non-volatile storage (EEPROM):
- FT232RL USB UART IC
  The I/O voltage of the FT232RL USB UART IC connections to the AMT49107 is set by the position of jumper J16 on the demonstration board:
  - □ J16 in the "5V" position sets the I/O voltage to 5 V.
  - □ J16 in the "3V3" position sets the I/O voltage to 3.3 V.

EQUIPMENT

Table 1: Equipment Required for Demonstration Board Logic I/O Voltage Change

Item	Description	Comment
1	AMT49107 Demonstration Board	Silk Screen Ident: EDC174
2	USB-A to USB-Micro-B Cable	–
3	AMT49107 Graphical User Interface (GUI)	Available at the Allegro software portal at registration.allegromicro.com/login
4	Bench Power Supply (DC)	Rated output voltage ≥ 24 V; Rated output current ≥ 50 mA
5	Oscilloscope or Voltmeter	–
6	PC	Microsoft Windows 7 or later, USB port available

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HOW TO CHANGE LOGIC I/O VOLTAGE CONFIGURATION

This section provides procedures needed to change the I/O voltage configuration of the APEK49107 and fitted AMT49107 gate driver IC. The equipment required to change the demonstration board logic I/O voltage is listed in Table 1. Use one of the two following procedures, as relevant to your system needs:

- "Change Logic I/O Level From 3.3 V to 5 V"
- "Change Logic I/O Level From 5 V to 3.3 V"

Change Logic I/O Level From 3.3 V to 5 V

This procedure applies to an APEK49107 board that is configured for operation in conjunction with 3.3 V logic systems (i.e., the default setting at the point of supply with VLM = 0) and is to be reconfigured for operation in conjunction with 5 V logic systems (i.e., VLM = 1).

1. Use the reference designations marked on the PCB component-side silk screen to confirm the demonstration board is configured as follows:

   □ J1, J2, J3, J8, and J9 are fitted.

   □ J4 is fitted to “VL-U2”.

   □ J16 is fitted to “3V3”.

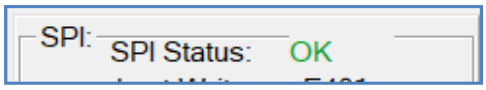
   □ J17, J18, J19, and J20 are fitted to “X8”.

   □ S1/1 through S1/3 are set to “OFF”.

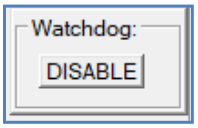
   □ S2/1 through S2/6 are set to “OFF”.

   All other jumper and switch states are not relevant to this procedure. However, additional notes about switch states, resistors, and voltages are provided in the "Additional Notes and Considerations" section.

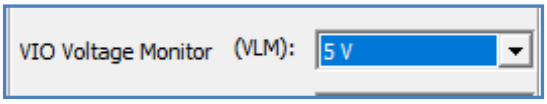
2. Connect X8 to a PC USB port with a standard USB-A to USB-Micro-B cable.
3. Connect the DC power supply to X2 (X2/1[VBAT] positive with respect to X2/2[GND]).
4. Adjust the DC power supply that is to be connected such that the voltage at the VBB terminal of U1 will comply with the non-volatile memory (NVM) programming voltage limit and the VBB functional operating range for the device, as specified in the product datasheet in effect—between 24 V (minimum) and 50 V (maximum), current limit ≥ 50 mA.
5. Turn on the power supply.
6. Run the AMT49107 GUI on the PC.
7. On the GUI, confirm the SPI Status at the top right of the main GUI is set to “OK”.



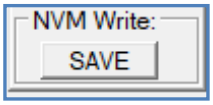
8. Set S1/1, S1/2, S1/3, and S2/1 to “ON”.
9. On the GUI, click on the <Watchdog: Disable> button.



10. Confirm the voltage on the SAL monitor pin is 3.3 V±0.5 V. (i.e., logic I/O is "3V3").
11. On the GUI:
    A. Click on the <BRIDGE AND SYSTEM> button.
    B. On the drop-down list, set the VIO Voltage Monitor (VLM) to “5V”.



    C. Close the <BRIDGE AND SYSTEM> window.
    D. Click on the <NVM Write: SAVE> button.



12. Set S1/1, S1/2, S1/3, and S2/1 to “OFF”.
13. Turn off the power supply.
14. Shut down the GUI.
15. Wait for at least 10 seconds.
16. Move J16 from “3V3” to “5V”.
17. Turn on the power supply.
18. Run the AMT49107 GUI on the PC.
19. On the GUI, confirm the SPI Status at the top right of the main GUI is set to “OK".
20. Set S1/1, S1/2, S1/3, and S2/1 to “ON”.
21. On the GUI, click on the <Watchdog: Disable> button.
22. Measure the voltage on the SAL monitor pin and confirm it is 5.0 V±0.5 V. (i.e., logic I/O is "5V").
23. Set S1/1, S1/2, S1/3, and S2/1 to “OFF”.
24. Turn off the power supply.
25. Shut down the GUI.

If the SAL voltage measured at Step 22 is 5.0 V±0.5 V, the board is now configured for 5 V logic I/O operation on every power up without further intervention. The demonstration board may be used as required.

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Change Logic I/O Level From 5 V to 3.3 V

This procedure applies to an APEK49107 board that is configured for operation in conjunction with 5 V logic systems (i.e., VLM = 1) and is to be reconfigured for operation in conjunction with 3.3 V logic systems (i.e., VLM = 0).

1. Use the reference designations marked on the PCB component-side silk screen to confirm the demonstration board is configured as follows:

   □ J1, J2, J3, J8, and J9 are fitted.

   □ J4 is fitted to “VL-U2”.

   □ J16 is fitted to “5V”.

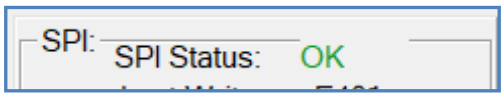
   □ J17, J18, J19, are J20 are fitted to “X8”.

   □ S1/1 through S1/3 are set to “OFF”.

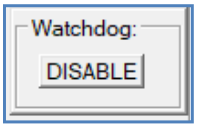
   □ S2/1 through S2/6 are set to “OFF”.

   All other jumper and switch states are not relevant to this procedure. However, additional notes about switch states, resistors, and voltages are provided in the "Additional Notes and Considerations" section.

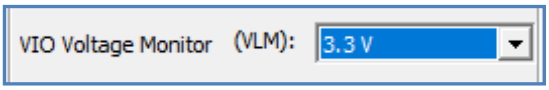
2. Connect X8 to a PC USB port with standard USB-A to USB-Micro-B cable.
3. Connect a DC power supply to X2 (X2/1[VBAT] positive with respect to X2/2[GND]).
4. Adjust the DC power supply that is to be connected such that the voltage at the VBB terminal of U1 will comply with the non-volatile memory (NVM) programming voltage limit and the VBB functional operating range for the device, as specified in the product datasheet in effect—between 24 V(minimum) and 50 V(maximum), current limit ≥ 50 mA.
5. Turn on the power supply.
6. Run the AMT49107 GUI on the PC.
7. On the GUI, confirm the SPI Status at the top right of the main GUI is set to “OK”.



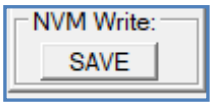
8. Set S1/1, S1/2, S1/3, and S2/1 to “ON”.
9. On the GUI, click on the <Watchdog: Disable> button.



10. Confirm the voltage on the SAL monitor pin is 5.0 V±0.5 V. (i.e., logic I/O is "5V").
11. On the GUI:
    A. Click on the <BRIDGE AND SYSTEM> button.
    B. On the drop-down list, set the VIO Voltage Monitor (VLM) to “5 V”; then re-set VLM to “3.3 V”.



    C. Close the <BRIDGE AND SYSTEM> window.
    D. Click on the <NVM Write: SAVE> button.



12. Set S1/1, S1/2, S1/3, and S2/1 to “OFF”.
13. Turn off the power supply.
14. Shut down the GUI.
15. Wait for at least 10 seconds.
16. Move J16 from “5V” to “3V3”.
17. Turn on the power supply.
18. Run the AMT49107 GUI on the PC.
19. On the GUI, confirm the SPI Status at the top right of the main GUI is set to “OK”.
20. Set S1/1, S1/2, S1/3, and S2/1 to “ON”.
21. On the GUI, click on the <Watchdog: Disable> button.
22. Measure the voltage on the SAL monitor pin and confirm it is 3.3 V±0.5 V (i.e., logic I/O is "3V3").
23. Set S1/1, S1/2, S1/3, and S2/1 to “OFF”.
24. Turn off the power supply.
25. Shut down the GUI.

If the SAL voltage measured at Step 22 is 3.3 V±0.5 V, the board is now configured for 3.3 V logic I/O operation on every power up without further intervention. The demonstration board may be used as required.

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ADDITIONAL NOTES AND CONSIDERATIONS

On-Board Linear Regulator

Linear regulator (U2) is a fixed-value, 5 V (nominal) output device. If any of the switches on S1 or S2 are closed, a 5 V (nominal) logic high is applied to the corresponding AMT49107 discrete control input:

- In the 5 V logic I/O configuration (VLM = 1), the applied logic high voltage is directly compatible with the discrete logic input high threshold of the AMT49107.
- In the 3.3 V logic I/O configuration (VLM = 0), the applied logic high voltage is compatible with the discrete logic input high threshold of the AMT49107, though the applied voltage exceeds the set logic I/O voltage for the part. This is acceptable because all logic inputs are 5 V logic level tolerant, regardless of the AMT49107 logic I/O voltage setting (5 V or 3.3 V).

If setting the AMT49107 for 3.3 V logic I/O operation and then connecting an external logic driver to any of the RESETn, POK, ENABLE, Hx, or Lx pins on connector X5, ensure that the 5 V generated by LDO U2 does not propagate to the externally connected logic driver:

- Set all switches on S1 and S2 corresponding to the driven pins to the "OFF" position; or
- Switch jumper J4 from the U2 position to the X3 position, and connect a suitable external 3.3 V DC supply to connector X3.

Resistors R27–35 and R43 limit any current flow from U2 or an external supply connected to X3 back into logic drivers connected to the RESETn, POK, ENABLE, Hx, or Lx pins on connector X5.

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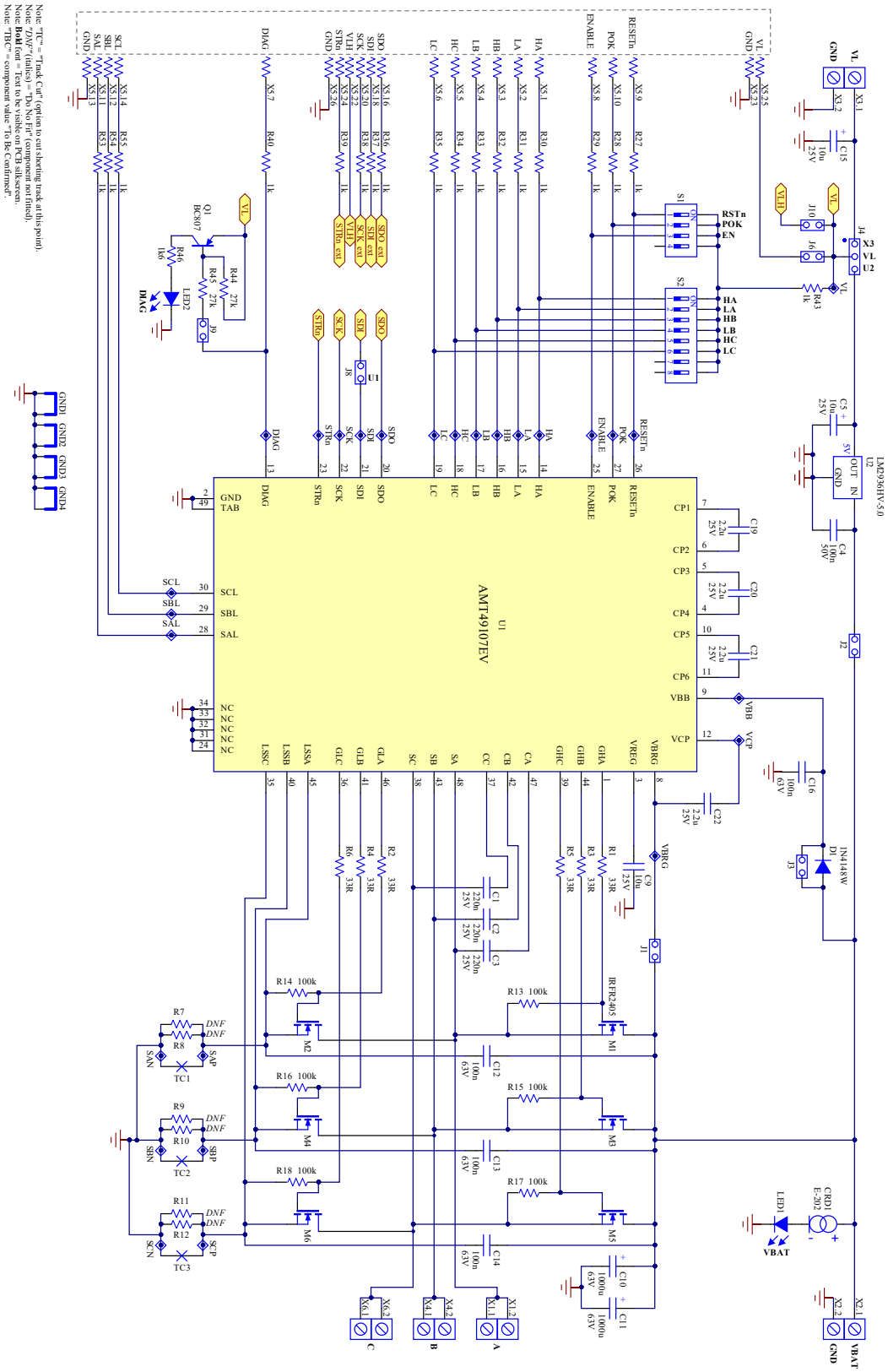
APPENDIX 1: AMT49107 DEMONSTRATION BOARD SCHEMATICS



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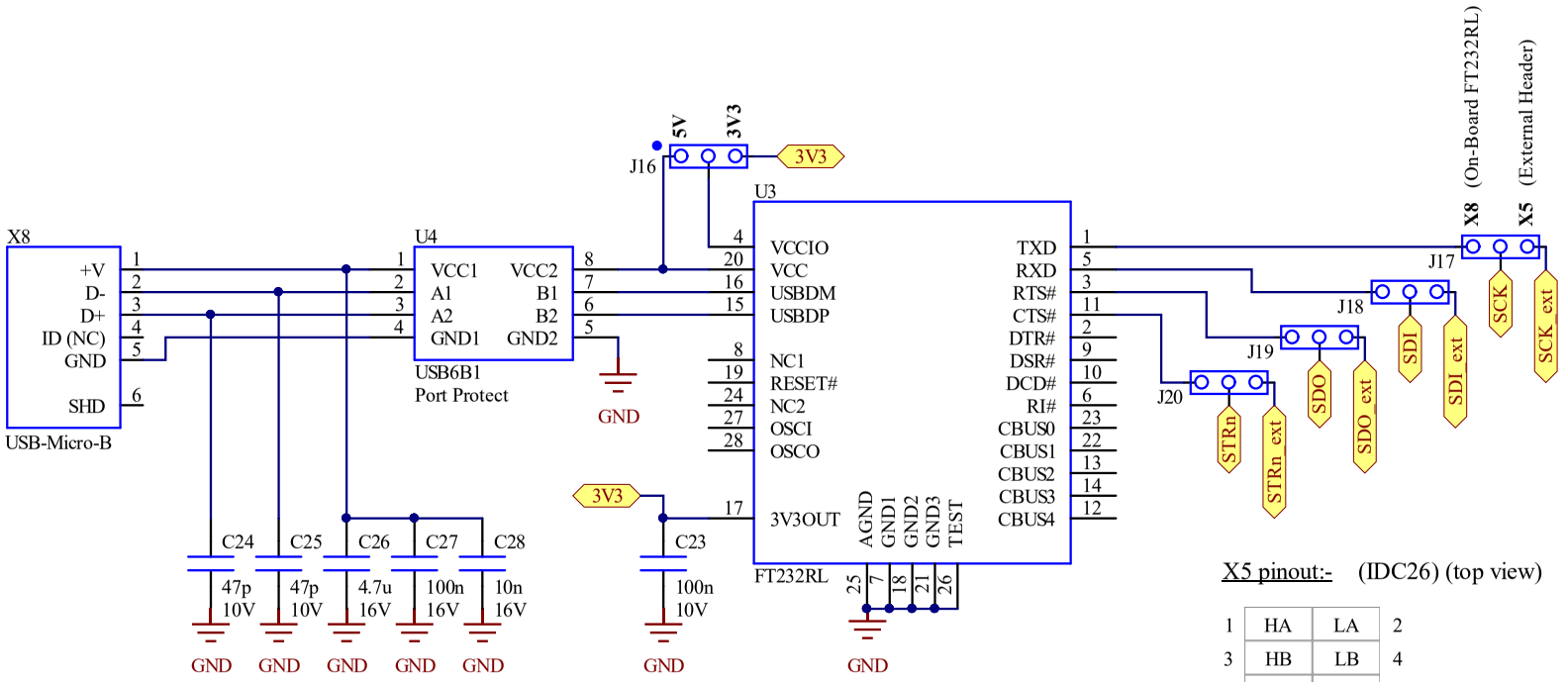

X5 pinout:- (IDC26) (top view)

1	HA	LA	2
3	HB	LB	4
5	HC	LC	6
7	DIAG	EN	8
9	RSTn	POK	10
11	SAL	SBL	12
13	GND	SCL	14
15		SDO	16
17		SDI	18
19		SCK	20
21		VLH	22
23	GND	STRn	24

SPI Cable

Green	
Yellow	
Orange	
Red	
Brown	

SPI over USB:-

If desired, an SPI cable (3V3 or 5V) can be used instead of the Micro-B-USB connector X8 and on-board FT232RL device (U3).

Move links on J17-J20, then connect the cable 6 pin socket to X5 header pins 16, 18, 20, 22, 24, and 25 as shown.

Revision History

Number	Date	Description
–	June 2, 2022	Initial release

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