Self-Powered Single-Channel Isolated GaNFET Driver with Regulated Bipolar Output Drive

FEATURES AND BENEFITS

- Power-Thru integrated isolated bias
  - □ No high-side bootstrap or external secondary-side bias
- Bipolar drive output, with adjustable regulated positive rail
- Regulated 3.3 V low power bias output
- 50 ns propagation delay, with excellent device-to-device matching of 5 ns
- Separate drive output pins: pull-up (2.8 Ω) and pull-down (1.0 Ω)
- Supply voltage 10.5 V < V_{DRV} < 13.2 V
- Undervoltage lockout on primary V_{DRV} and secondary V_{SEC}
- Enable pin with fast response
- Overtemperature protection
- CMTI > 100 V/ns dv/dt immunity
- Creepage distance > 8 mm
- Distance-through-insulation DTI ≥ 450 µm
- Safety regulatory approvals (pending)
  - □ 5.7 kV RMS V_{ISO} per UL 1577
  - □ 8 kV pk V_{IOTM} maximum transient isolation voltage per VDE0884-11
  - □ 630 V pk maximum working isolation voltage

APPLICATIONS

- **AC-DC and DC-DC converters**: Totem-pole PFC, LLC half-/full-bridge, SR drive, multi-level converters, phase-shifted full-bridge
- **Automotive**: OBC, traction drive
- **Industrial**: transportation, robotics
- **Grid Infrastructure**: micro-inverters, solar

DESCRIPTION

The AHV85111 isolated gate driver is optimized for driving GaNFETs in multiple applications. An isolated dual positive/negative output bias supply is integrated into the driver device, eliminating external gate drive auxiliary bias supply or high-side bootstrap. The bipolar output rails with adjustable and regulated positive rail improves dv/dt immunity, greatly simplifies the system design, and reduces EMI through reduced total common-mode (CM) capacitance. It also allows the driving of a floating switch in any location in a switching power topology.

The driver has fast propagation delay and high peak source/sink capability to efficiently drive GaNFETs in high-frequency designs. High CMTI combined with isolated outputs for both bias power and drive make it ideal in applications requiring isolation, level-shifting, or ground separation for noise immunity.

The device is available in a compact low-profile surface-mount NH package. Several protection features are integrated, including undervoltage lockout on primary and secondary bias rails, internal pull-down on IN pin and OUTPD pin, fast response enable input, and overtemperature shutdown.

PACKAGE

Not to scale

10 mm × 7.66 mm × 2.53 mm
12-pin low-profile surface mount

TYPICAL APPLICATION

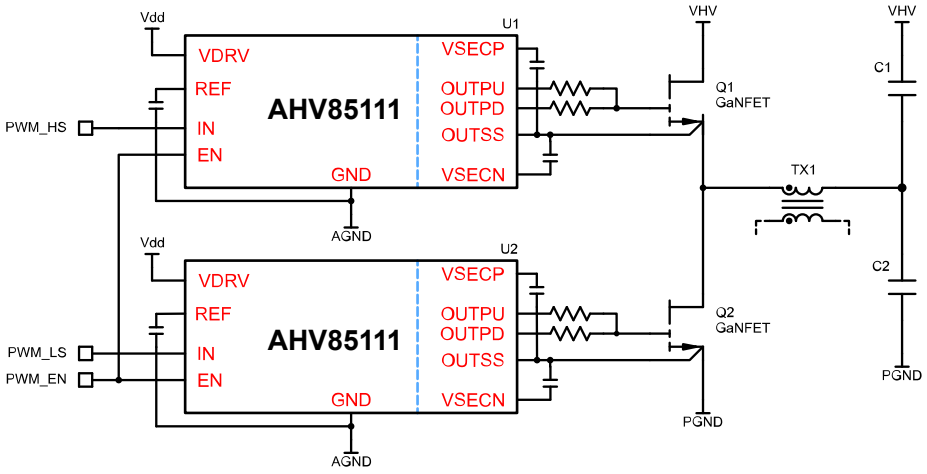

Figure 1: Typical AHV85111 half-bridge application—eliminates high-side bootstrap

SELECTION GUIDE

Part Number	Switch	# of Channels	Output	Isolation	Package
AHV85111KNHTR	GaN Driver	1	Unipolar	Isolated	10 mm × 7.66 mm × 2.53 mm 12-pin low-profile surface mount

ABSOLUTE MAXIMUM RATINGS [1]

Characteristic	Symbol	Notes	Rating	Unit
Drive Supply Voltage	V_{DRV}	VDRV, wrt to GND	V_{GND} – 0.5 to 15	V
Input Data	V_{IN}	IN, wrt to GND	V_{GND} – 0.5 to 15	V
Enable	V_{EN}	EN, wrt to GND	V_{GND} – 0.5 to 15	V
Select	V_{SEL}	SEL to GND; internal use only	V_{GND} – 0.5 to 15	V
Reference Voltage	V_{REF}	3.3 V reference, wrt GND	V_{GND} – 0.5 to 4	V
Output Drive Pull-Up	V_{OUTPU}	OUTPU to OUTSS	V_{SECN} – 0.5 to 15	V
Output Drive Pull-Down	V_{OUTPD}	OUTPU to OUTSS	V_{SECN} – 0.5 to 15	V
Isolated Bias Supply	$V_{SECP} – V_{SECN}$	Total rail	–0.5 to 15	V
Junction Temperature	T_J		–40 to 150	°C

[1] Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

VSECP AND VSECN PIN CAPACITORS: –40°C < T_J< 125°C, 10.5 V < V_{DRV} < 13.2 V, $C_{SEC(NET)}$ = 22 nF, C_{out} = 1 nF, unless otherwise stated. Note that $C_{SEC(NET)}$ is the net equivalent of C_{SECP} in series with C_{SECN}, i.e. (C_{SECP} × C_{SECN}) / (C_{SECP} + C_{SECN}).

Characteristic	Symbol	Test Conditions	Min.	Typ. [3]	Max.	Unit
VSEC Pin Capacitor CSEC	C_{SECP}	External capacitance connected between VSECP and OUTSS pins; external C_{OUT} = 1 nF	5 [1]	27	100 [1]	nF
	C_{SECN}	External capacitance connected between VSECN and OUTSS pins; external C_{OUT} = 1 nF	15 [1]	100	330 [1]	nF

[1] Smaller C_{SEC} values than the recommended typical value can give higher voltage ripple on CSEC.
[2] Larger C_{SEC} values will mean longer startup times.
[3] Typical values should be chosen to match the ratio of V_{SECP} to V_{SECN}.

ESD RATINGS

Characteristic	Symbol	Test Conditions	Value	Unit
Human Body Model	V_{HBM}		±2	kV
Charged Device Model	V_{CDM}		±500	V

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions*	Value	Unit
Junction-to-Ambient Thermal Resistance	$R_{\theta JA}$		*TBD*	°C/W
Junction-to-Case Thermal Resistance	$R_{\theta JC}$		*TBD*	°C/W

*Additional thermal information available on the Allegro website.

Advance Information Datasheet
Subject to Change Without Notice
August 30, 2022

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Revision History

Number	Date	Description
–	August 30, 2022	Initial release

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