

Coreless, High Precision, Hall-Effect Current Sensor IC with Common-Mode Field Rejection, Overcurrent and Overtemperature Detection

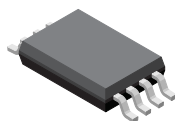
FEATURES AND BENEFITS

- Eliminates need for concentrator core or shield
- Contactless, lossless, non-invasive current sensing
- Suited for applications where current flows through busbar or PCB
- High operating bandwidth: DC to 250 kHz
- Overcurrent (OCF) and Overtemperature (OTF) detection on Fault Pin
- Differential Hall sensing rejects common-mode magnetic fields
- Very fast response time ($<2 \mu\text{s}$ typ)
- Wide sensing range (3 to 28 mV/G)
 - Ideal for sensing currents from 100 A to >4000 A
- Factory-programmed segmented linear temperature compensation (TC) provides low thermal drift
 - Sensitivity $\pm 1\%$ (typ)
 - Offset ± 3 mV (typ)
- Customer-programmable, high-resolution offset and sensitivity trim
- Wide Hall elements spacing for improved SNR and thermal performance
- Ultra-sensitive Hall elements for improved noise performance

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PACKAGE:

8-pin TSSOP package (suffix LU)



Not to scale

DESCRIPTION

The Allegro ACS37610 current sensor IC enables low-cost solutions for AC and DC current sensing without the need for an external field concentrator core or a U-shaped magnetic shield. It is designed for applications where hundreds or thousands of amps flow through a busbar or PCB.

Current flowing through a busbar or PCB trace generates a magnetic field that is sensed by the monolithic, low-offset, linear Hall IC. The differential sensing topology virtually eliminates all types of errors due to common-mode stray magnetic fields. The wide spacing between the differential Hall elements (2.58 mm) coupled with the increased sensitivity of each Hall element enable the ACS37610 to achieve superior signal to noise (SNR) and improved resolution. While not mandatory, a notch or slit in the current-carrying busbar or PCB copper trace provides further improvements to the system's SNR. High isolation is achieved via the no-contact nature of this simple assembly.

The ACS37610 is offered with regular and low-power mode, enabling customers to achieve optimal SNR and power consumption. A dedicated user-programmable overcurrent and overtemperature fault pin, and a slew of built-in diagnostics, including broken ground and VCC detection, make it ideal for

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TYPICAL APPLICATIONS

- High voltage traction motor inverter
- 48 V / 12 V auxiliary inverter
- Heterogeneous redundant battery monitoring
- Overcurrent detection
- DC/DC converter
- Smart fuse
- Power distribution unit (PDU)
- Power supply

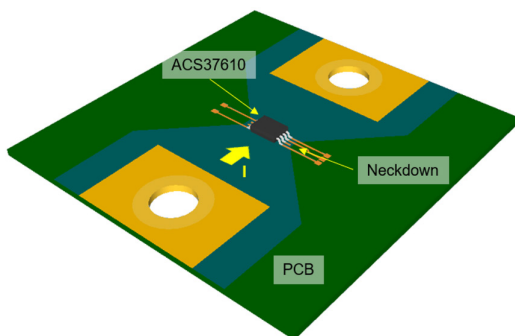


Figure 1: Current Through PCB

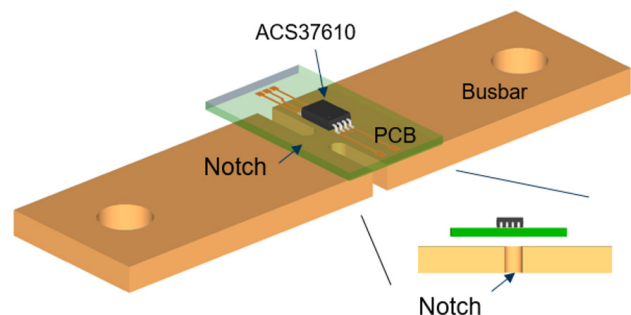


Figure 2: Current Through Busbar

ACS37610

Coreless, High Precision, Hall-Effect Current Sensor IC with Common-Mode Field Rejection, Overcurrent and Overtemperature Detection

FEATURES AND BENEFITS (continued)

- Wide ambient temperature range: -40°C to 150°C
- 3.3 or 5.0 V single supply operation
- Programmable through Output pin or through dedicated Programming pin for easier device programming
- AEC-Q100 Grade 0, automotive qualified
- Monolithic Hall IC for high reliability
- Surface mount, small footprint, low-profile TSSOP8 package

DESCRIPTION (continued)

safety-critical applications. The accuracy and flexibility of this device is enhanced by user programmability, performed via the output pin or through the dedicated programming pin, which allows the device to be optimized in the application and cancels errors due to mechanical assembly tolerances on the PCB. Device specifications apply across an extended ambient temperature range: -40°C to 150°C .

The ACS37610 is suitable for space-constrained applications because of its low-profile 8-pin surface mount TSSOP package (thin-shrink small outline package, suffix LU) that is lead (Pb) free, with 100% matte tin leadframe plating. The sensor can be mounted in a horizontal or vertical orientation relative to the busbar, providing superior flexibility in mechanical assemblies.

SELECTION GUIDE

Part Number	Nominal Supply Voltage (V)	Differential Magnetic Input Range, (G)	Sensitivity Sens (Typ.) (mV/G) ^[1]	Sensitivity Trim Range (mV/G) ^[1]	T _A (°C)	Packing ^[2]
ACS37610LLUATR-005B5	5	± 400	5	3 to 7	-40 to 150	4000 pieces per 13-inch reel
ACS37610LLUATR-010B5	5	± 200	10	6 to 14		
ACS37610LLUATR-020B5	5	± 100	20	12 to 28		
ACS37610LLUATR-020U5	5	0 to 200	20	12 to 28		
ACS37610LLUATR-010B3	3.3	± 132	10	6 to 14		

^[1] Measured at nominal supply voltage. Contact Allegro for other sensitivity options.

^[2] Contact Allegro for additional packing options.

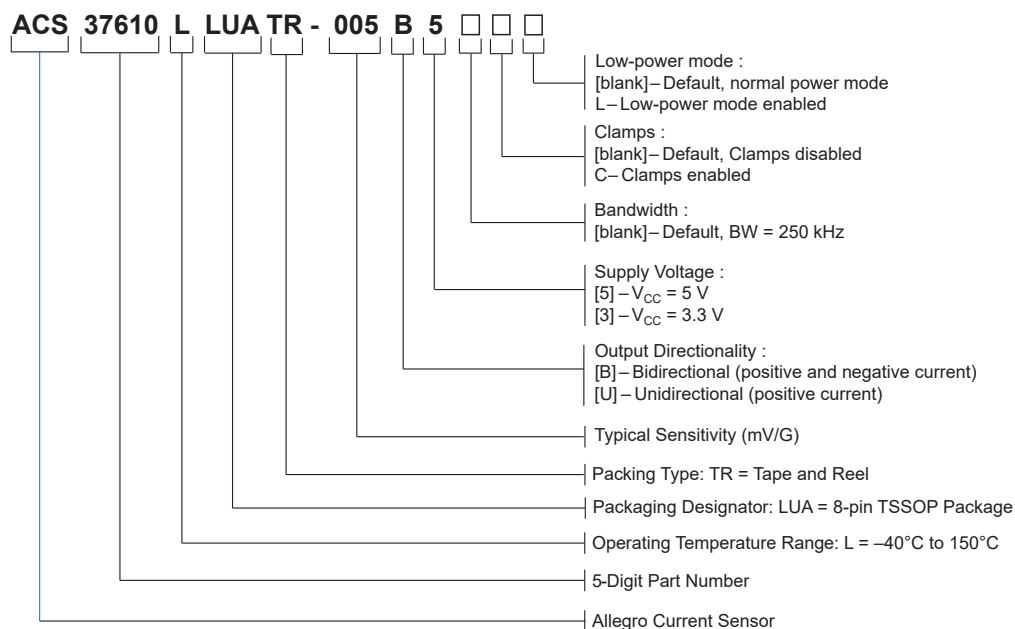


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ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{CC}	For a maximum duration of 1 minute	7.5	V
Reverse Supply Voltage	V_{RCC}		-0.5	V
Output Voltage	V_{OUT}		6.5	V
Reverse Output Voltage	V_{ROUT}		-0.5	V
Fault Voltage	V_F		6.5	V
Reverse Fault Output Voltage	V_{FR}		-0.5	V
Output Source Current	$I_{OUT(SOURCE)}$	VOUT to GND	25	mA
Output Sink Current	$I_{OUT(SINK)}$	Maximum survivable sink or source current on the output	10	mA
Nominal Operating Ambient Temperature	T_A	Range L	-40 to 150	°C
Maximum Junction Temperature	$T_{J(max)}$		165	°C
Storage Temperature	T_{stg}		-65 to 165	°C

ESD RATINGS

Characteristic	Symbol	Test Conditions	Value	Unit
Human Body Model	V_{HBM}	Per JEDEC JS-001	9	kV
Charged Device Model	V_{CDM}	Per JEDEC JS-002	1	kV

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions [1]	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	TSSOP-8 on 4-layer PCB based on JEDEC standard	145	°C/W

[1] Additional thermal information available on the Allegro website.

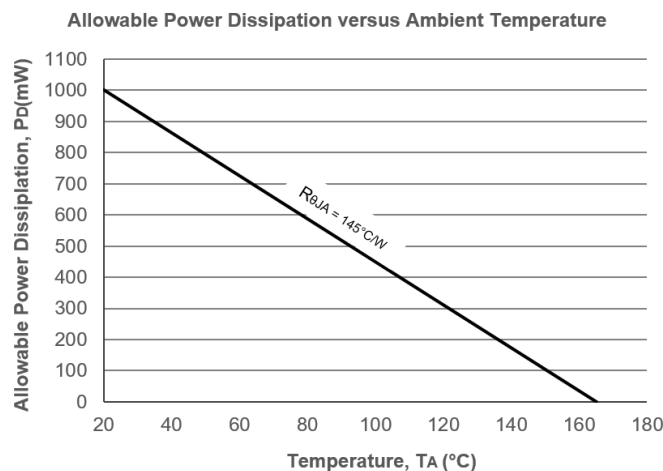
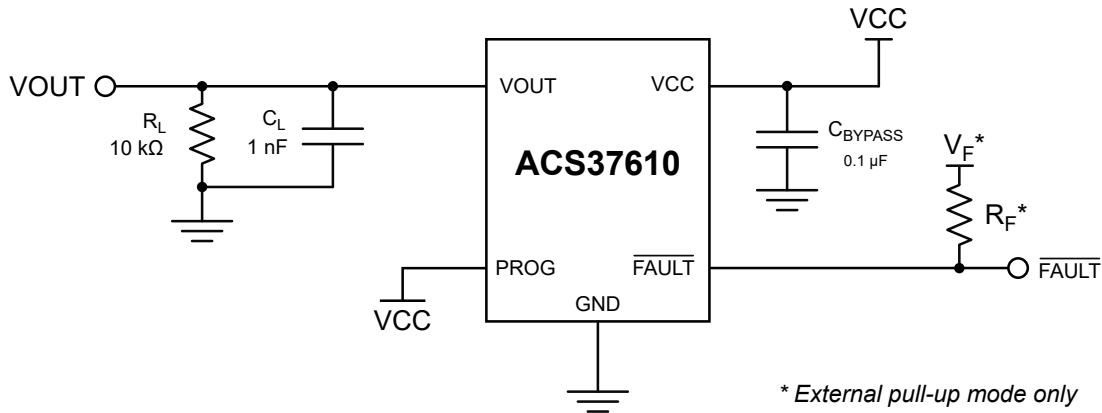
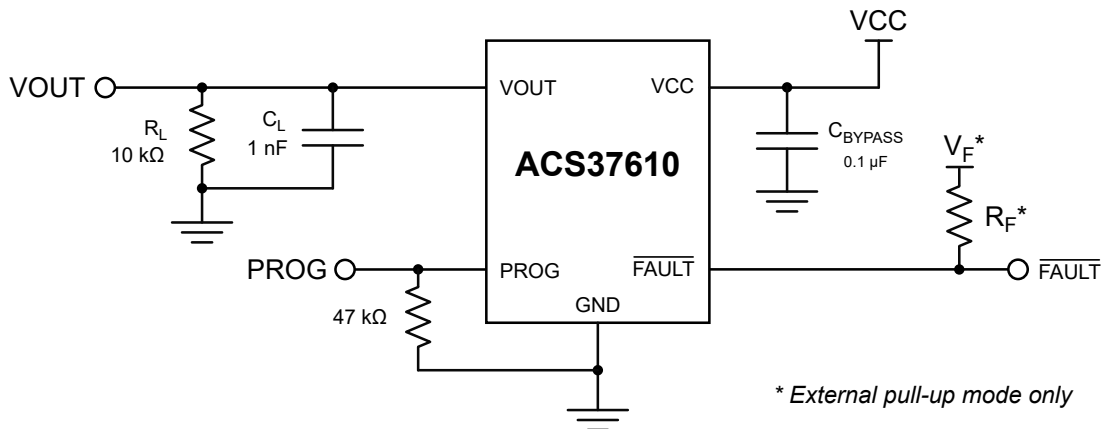


Figure 3: Allowable Power Dissipation

TYPICAL APPLICATION CIRCUITS



**Figure 4: Typical Application Circuit
(Programming Pin Not Used)**



**Figure 5: Typical Application Circuit
(Programming Pin Used)**

The ACS37610 outputs an analog signal, V_{OUT} , that varies linearly with the bidirectional AC or DC field sensed, within the range specified. C_L is for optimal noise management, with values that depend on the application. R_L is an optional pulldown to GND or pullup to VCC for broken wire detection. For broken GND function, it is recommended to tie PROG pin to VCC when not used. R_F is an optional pull-up resistor to V_F , to be used when disabling the device internal pull-up in memory.

PINOUT DIAGRAM AND PINOUT LIST

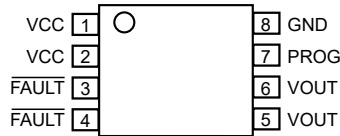


Figure 6: Pinout Diagram

Pinout List

Number	Name	Description
1,2	VCC	Input power supply; also used for programming
3,4	FAULT	Fault output; overcurrent, overtemperature
5,6	VOUT	Analog output signal; also used for programming
7	PROG	Bidirectional programming pin
8	GND	Ground pin

FUNCTIONAL BLOCK DIAGRAM

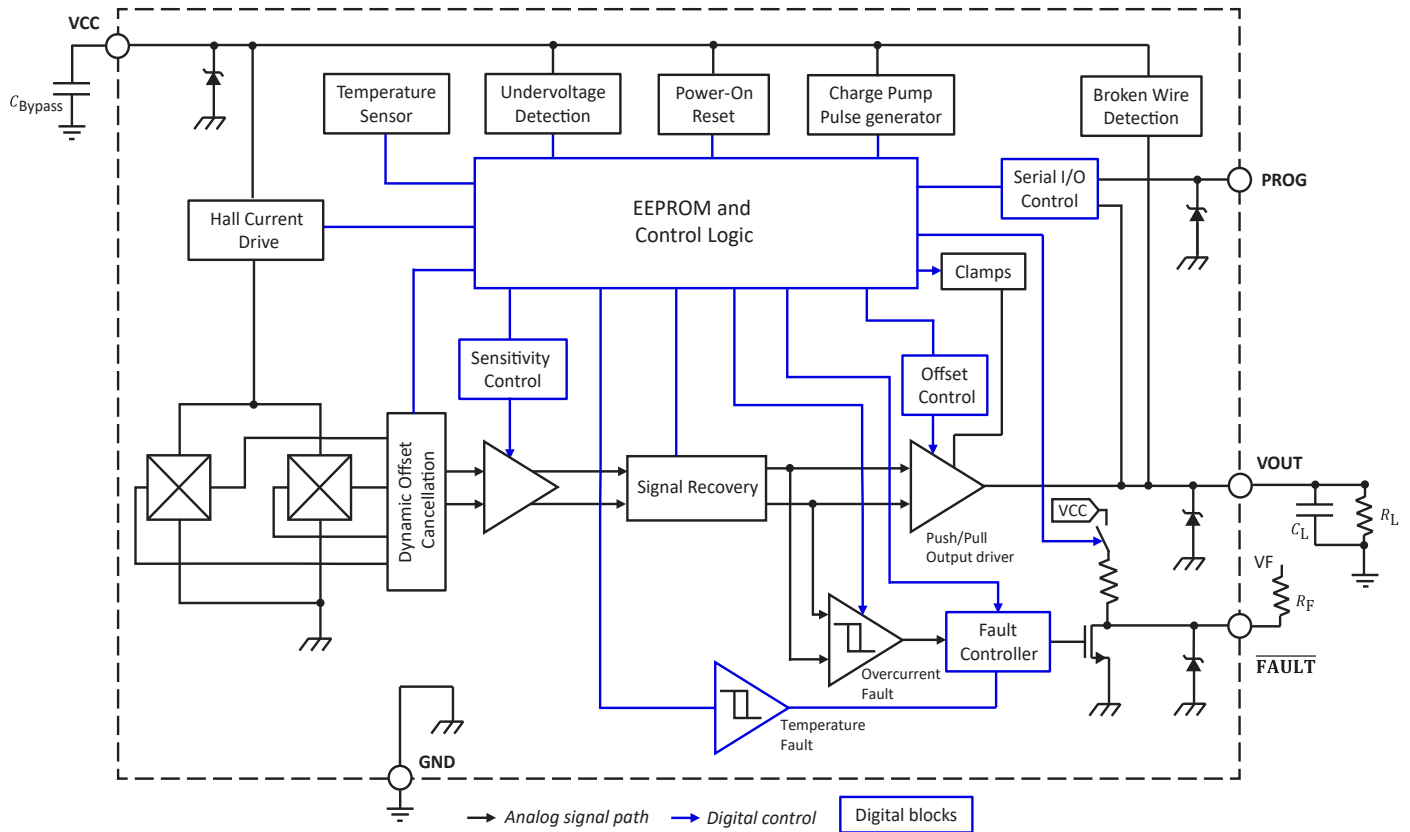


Figure 7: Functional Block Diagram

COMMON OPERATING CHARACTERISTICS: Valid through full range of T_A and V_{CC} , $C_{BYPASS} = 100$ nF, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
ELECTRICAL CHARACTERISTICS						
Supply Voltage	V_{CC}	5 V nominal supply voltage variant	4.5	5	5.5	V
		3.3 V nominal supply voltage variant	3	3.3	3.6	V
Supply Current	I_{CC}	5 V nominal supply voltage variant; $V_{CC}(\min) \leq V_{CC} \leq V_{CC}(\max)$, no load on output	–	16.5	21	mA
		5 V nominal supply voltage variant; low-power mode, no load on output	–	13.5	18	mA
		3.3 V nominal supply voltage variant; $V_{CC}(\min) \leq V_{CC} \leq V_{CC}(\max)$, no load on output	–	14.5	19	mA
		3.3 V nominal supply voltage variant; low-power mode, no load on output	–	10.5	14	mA
Power-On Time	t_{PO}	$T_A = 25^\circ\text{C}$, C_L (of test probe) = 10 pF, $C_{BYPASS} = \text{open}$	–	70	–	μs
Temperature Compensation Power-On Time	t_{TC}	Time after Power-On Time (t_{PO}) required to get valid temperature-compensated output; $T_A = 150^\circ\text{C}$, $C_{BYPASS} = \text{open}$, $C_L = 1$ nF	–	45	–	μs
Fault Power-On Time	$t_{PO(\text{FAULT})}$	Time from when $V_{CC} > V_{UVLOD}$ to when OCF will react to overcurrent event	–	270	–	μs
Overvoltage Detection Threshold	V_{OVDE}	$T_A = 25^\circ\text{C}$, V_{CC} rising and device function disabled	6.35	6.9	7.2	V
	V_{OVDD}	$T_A = 25^\circ\text{C}$, V_{CC} falling and device function enabled	5.75	6	6.25	V
	V_{OVHYS}	$T_A = 25^\circ\text{C}$	–	450	–	mV
OVD Enable/Disable Delay Time	t_{OVDE}	$T_A = 25^\circ\text{C}$, $C_{BYPASS} = \text{open}$, $C_L = 1$ nF	–	60	–	μs
	t_{OVDD}	$T_A = 25^\circ\text{C}$, $C_{BYPASS} = \text{open}$, $C_L = 1$ nF	–	3	–	μs
Undervoltage Lockout (UVLO) Threshold	V_{UVLOD}	V_{CC} rising, 5 V variant only	–	4.1	4.3	V
	V_{UVLOE}	V_{CC} falling, 5 V variant only	3.45	3.75	–	V
Undervoltage Lockout (UVLO) Hysteresis	$V_{UVLO(\text{HYS})}$	5 V variant only	–	450	–	mV
UVD Enable/Disable Delay Time	t_{UVLOE}	Time measured from falling $V_{CC} < V_{UVLOE}$ to UVLO enabled; $T_A = 25^\circ\text{C}$, $C_{BYPASS} = \text{open}$, $C_L = 1$ nF	–	65	–	μs
	t_{UVLOD}	Time measured from rising $V_{CC} > V_{UVLOD}$ to UVLO disabled; $T_A = 25^\circ\text{C}$, $C_{BYPASS} = \text{open}$, $C_L = 1$ nF	–	8	–	μs
Power-On Reset Voltage	V_{PORH}	V_{CC} rising	2.7	2.9	3	V
	V_{PORL}	V_{CC} falling	2.5	2.7	2.9	V
Power-On Reset Hysteresis	$V_{HYS(\text{POR})}$		50	150	–	mV
Power-On Reset Release Time	t_{PORR}	Time V_{CC} must be held above V_{PORH} to start counting for t_{UVLOD} after $V_{CC} > V_{UVLOD}$ and transition from high impedance to normal operation; $T_A = 25^\circ\text{C}$, V_{CC} rising	–	65	–	μs
Internal Bandwidth [1]	BW_i	–3 dB, $C_L = 1$ nF, $T_A = 25^\circ\text{C}$	–	250	–	kHz
Rise Time [1]	t_r	$T_A = 25^\circ\text{C}$, $C_L = 1$ nF, 1 V step on output, $BW_i = 250$ kHz	–	2.4	–	μs

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COMMON OPERATING CHARACTERISTICS (continued): Valid through full range of T_A and V_{CC} . $C_{BYPASS} = 100$ nF, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Propagation Delay [1]	t_{PD}	$T_A = 25^\circ\text{C}$, $C_L = 1$ nF, 1 V step on output, $BW_i = 250$ kHz	–	1.1	–	μs
Response Time [1]	$t_{RESPONSE}$	$T_A = 25^\circ\text{C}$, $C_L = 1$ nF, 1 V step on output, $BW_i = 250$ kHz	–	1.6	–	μs
DC Output Impedance	R_{OUT}		–	< 1	–	Ω
Output Load Resistance	R_L	VOU to GND	4.7	10	–	k Ω
Output Load Capacitance	C_L	VOU to GND	–	1	10	nF
Delay to Clamp	t_{CLP}	$T_A = 25^\circ\text{C}$; $C_L = 1$ nF; Step from 75% output range to 150%	–	5	–	μs
Output Full-Scale Range	$V_{OUT(FSR)}$	Full-scale output, 5 V variant, bidirectional	–	± 2	–	V
		Full-scale output, 3.3 V variant, bidirectional	–	± 1.32	–	V
		Full-scale output, 5 V variant, unidirectional	–	4	–	V
Output Voltage Clamp	$V_{CLP(HIGH)}$	$V_{CC} = 5$ V, $R_{L(PULLDOWN)} = 10$ k Ω to GND	4.48	–	4.75	V
		$V_{CC} = 3.3$ V, $R_{L(PULLDOWN)} = 10$ k Ω to GND	2.94	–	3.18	V
	$V_{CLP(LOW)}$	$V_{CC} = 5$ V, $R_{L(PULLUP)} = 10$ k Ω to VCC	0.25	–	0.5	V
		$V_{CC} = 3.3$ V, $R_{L(PULLUP)} = 10$ k Ω to VCC	0.15	–	0.33	V
Output Saturation Voltage	$V_{SAT(HIGH)}$	$R_{L(PULLDOWN)} = 10$ k Ω to GND	$V_{CC} - 0.2$	–	–	V
	$V_{SAT(LOW)}$	$R_{L(PULLUP)} = 10$ k Ω to VCC	–	–	200	mV
Broken Wire Voltage	$V_{BRK(High)}$	$R_{L(PULLUP)} = 10$ k Ω to VCC	$V_{CC} - 0.1$	V_{CC}	V_{CC}	V
	$V_{BRK(Low)}$	$R_{L(PULLDOWN)} = 10$ k Ω to GND	0	0	100	mV
ERROR COMPONENTS						
Clamp Ratiometry Error	Rat_{ERRCLP}	$V_{CC} = \pm 3\%$ variation of nominal supply voltage	–	< ± 0.5	–	%
Common Mode Field Rejection Ratio	CMFRR	Measured at 100 G uniform magnetic field	–	40	–	dB
Noise Density	B_{ND}	Normal power mode, 5 V / 3.3 V variant, $T_A = 25^\circ\text{C}$, $C_L = 1$ nF	–	0.9	–	mG / $\sqrt{\text{Hz}}$
		Low-power mode, 5 V / 3.3 V variant, $T_A = 25^\circ\text{C}$, $C_L = 1$ nF	–	1.2	–	mG / $\sqrt{\text{Hz}}$

[1] Timing specified does not include potential effect of skin effect on conductor; value will depend on busbar/PCB design.

FAULT CHARACTERISTICS

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Positive Field Fault Switch Point Range [1]	OCF_PThres	Programmable using OCF positive threshold bits. In percent of full-scale positive output (2.5 to 4.5 V) on bidirectional variant.	50	–	200	%FS(+)
		Programmable using OCF positive threshold bits. In percent of full-scale output (0.5 to 4.5 V) on unidirectional variant.	50	–	200	%FS
Negative Field Fault Switch Point Range [1]	OCF_NThres	Programmable using OCF negative threshold bits. In percent of full-scale negative output (2 V typical, 2.5 to 0.5 V) on bidirectional variant	50	–	200	%FS(-) %FS
Overcurrent Fault Switch Point Step Size	OCF_step	Overcurrent fault threshold programming step size	–	1.6	–	%FS
Overcurrent Fault Accuracy	OCF_acc	Overcurrent fault threshold accuracy through full range of T_A	–5	±2	+5	%FS
Overcurrent Fault Response Time	t_{OCF}	$R_{F(PULLUP)} = 10\text{ k}\Omega$ from FAULT to VF, VOUT step from $V_{OUT(Q)}$ to $V_{OUT} = (V_{OUT(Q)} + OCF_PThres [V])$; $BW_i = 250\text{ kHz}$, OCF qualifier = 0	–	2.5	–	μs
Overtemperature Fault Sampling Rate	OTFs	Rate at which the temperature is sampled	–	8	–	ms
Fault Clear Time	$t_{C(F)}$	Time to release FAULT pin (go back to VF) when fault condition is no longer present. $R_F = 10\text{ k}\Omega$, external 100 pF from FAULT to VCC	–	8	–	μs
		Time to release FAULT pin (go back to VCC) when fault condition is no longer present. Internal fault pull-up enabled	–	15	–	μs
Fault Jitter	OCF_Jitt	$T_A = 25^\circ\text{C}$, 1 sigma	–	100	–	ns
Overcurrent Fault Hysteresis Level Range [1]	OCF_Hyst	Hysteresis in percent of trip level, $T_A = 25^\circ\text{C}$, OCF_Hyst = 0	–	11	–	%
		Hysteresis in percent of trip level, $T_A = 25^\circ\text{C}$, OCF_Hyst = 1	–	22	–	%
		Hysteresis in percent of trip level, $T_A = 25^\circ\text{C}$, OCF_Hyst = 2	–	45	–	%
		Hysteresis in percent of trip level, $T_A = 25^\circ\text{C}$, OCF_Hyst = 3	–	75	–	%
Overtemperature Fault Accuracy [1]	OTF_acc		–10	±3	+10	$^\circ\text{C}$
Overtemperature Fault Threshold Range [1]	OTF_thresh		80	160	165	$^\circ\text{C}$
Overtemperature Fault Step size			–	7	–	$^\circ\text{C}$
Overtemperature Fault Hysteresis [1]	OTF_Hyst	Overtemperature fault fixed hysteresis value	10	15	20	$^\circ\text{C}$
FAULT Pin Low Output Voltage	V_{FAULT}	$R_{F(PULLUP)} = 4.7\text{ k}\Omega$ from FAULT to VCC	–	–	0.4	V
FAULT Pin Leakage Current	I_{FLeak}	$R_{F(PULLUP)} = 4.7\text{ k}\Omega$ from FAULT to VCC	–	–	1.3	μA
External Pull-Up Supply Voltage [1]	$V_{F(PULLUP)}$		1.65	V_{CC}	V_{CC}	V
External FAULT Pullup Resistor [1]	$R_{F(PULLUP)}$		4.7	–	500	k Ω
External FAULT Capacitance [1]	C_F		–	–	10	nF
Internal FAULT Pull-Up Resistor	$R_{IF(PULLUP)}$	Internal pull up to V_{CC} ; set FaultR_dis bit to 1 in EEPROM to disable.	–	10	–	k Ω

[1] Limits guaranteed by design and characterization data, not tested in production.

-005B5 PERFORMANCE CHARACTERISTICS: Valid over full range of T_A and $V_{CC} = 5\text{ V}$, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
NOMINAL PERFORMANCE						
Differential Magnetic Range	B_{DIFF}	Corresponding full-scale magnetic range based on typical sensitivity	-400	-	400	G
Initial Factory-Programmed Sensitivity	Sens	Factory-programmed sensitivity; $T_A = 25^\circ\text{C}$	4.925	5	5.075	mV/G
Initial Quiescent Output Voltage	$V_{OUT(Q)}$	Factory-programmed quiescent output voltage; $T_A = 25^\circ\text{C}$	2.495	2.5	2.505	V
Noise [1]	V_N	$T_A = 25^\circ\text{C}$, $C_L = 1\text{ nF}$, $BW_i = 250\text{ kHz}$, initial sensitivity	-	2.8	-	mV _{RMS}
Nonlinearity	E_{LIN}	Tested up to full-scale output	-0.55	± 0.15	0.55	%
SENSITIVITY ERROR						
Sens Ratiometry Error [2]	$Rat_{ErrSens}$	$V_{CC} = \pm 3\%$ variation of nominal supply voltage	-0.75	± 0.25	0.75	%
Sensitivity Drift Over Temperature	$\Delta Sens_{TC}$	$T_A = 25^\circ\text{C}$ to 150°C , up to $\pm 40\%$ of sensitivity change	-1.5	± 1	1.5	%
		$T_A = -40^\circ\text{C}$ to 25°C , up to $\pm 40\%$ of sensitivity change	-1.5	± 1	1.5	%
QUIESCENT VOLTAGE OUTPUT ERROR						
QVO Ratiometry Error [2]	$V_{RatErrQVO}$	$V_{CC} = \pm 3\%$ variation of nominal supply voltage	-5	± 2	5	mV
Quiescent Voltage Output Temperature Error	$V_{OUT(Q)TC}$	$T_A = 25^\circ\text{C}$ to 150°C , up to $\pm 40\%$ of sensitivity change	-5	± 3	5	mV
		$T_A = -40^\circ\text{C}$ to 25°C , up to $\pm 40\%$ of sensitivity change	-5	± 3	5	mV
LIFETIME DRIFT CHARACTERISTICS [3]						
QVO Lifetime Drift	$V_{OUT(Q)LIFE}$	Initial sensitivity	-	± 4.7	-	mV
Sens Lifetime Drift	$Sens_{LIFE}$	Initial sensitivity	-	± 0.75	-	%
Additional QVO Temperature Error Relative to 25°C Due to Lifetime		$T_A = -40^\circ\text{C}$ to 150°C , initial sensitivity	-	1.1	-	mV
Additional Sensitivity Error Relative to 25°C Due to Lifetime		$T_A = -40^\circ\text{C}$ to 150°C , initial sensitivity	-	0.1	-	%

[1] Noise scales with sensitivity.

[2] For lower V_{CC} variations than test conditions, Ratiometry Error linearly scales with V_{CC} , e.g. $\pm 1.5\%$ variations on V_{CC} instead of $\pm 3\%$ leads to $Rat_{ErrSens}$ and $V_{RatErrQVO}$ to be divided by 2.

[3] Lifetime drift characteristics are based on the AEC-Q100 qualification results from zero-hour reads. Typical values are the worst-case observed drift, ± 3 sigma, during AEC-Q100 qualification from any of the -40°C , 25°C , or 150°C temperatures.

-010B5 PERFORMANCE CHARACTERISTICS: Valid over full range of T_A and $V_{CC} = 5\text{ V}$, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
NOMINAL PERFORMANCE						
Differential Magnetic Range	B_{DIFF}	Corresponding full-scale magnetic range based on typical sensitivity	-200	-	200	G
Initial Factory-Programmed Sensitivity	Sens	Factory-programmed sensitivity; $T_A = 25^\circ\text{C}$	9.85	10	10.15	mV/G
Initial Quiescent Output Voltage	$V_{OUT(Q)}$	Factory-programmed quiescent output voltage; $T_A = 25^\circ\text{C}$	2.495	2.5	2.505	V
Noise [1]	V_N	$T_A = 25^\circ\text{C}$, $C_L = 1\text{ nF}$, $BW_i = 250\text{ kHz}$, initial sensitivity	-	5	-	mV _{RMS}
Nonlinearity	E_{LIN}	Tested up to full-scale output	-0.55	± 0.15	0.55	%
SENSITIVITY ERROR						
Sens Ratiometry Error [2]	$Rat_{ErrSens}$	$V_{CC} = \pm 3\%$ variation of nominal supply voltage	-0.75	± 0.25	0.75	%
Sensitivity Drift Over Temperature	$\Delta Sens_{TC}$	$T_A = 25^\circ\text{C}$ to 150°C , up to $\pm 40\%$ of sensitivity change	-1.5	± 1	1.5	%
		$T_A = -40^\circ\text{C}$ to 25°C , up to $\pm 40\%$ of sensitivity change	-1.5	± 1	1.5	%
QUIESCENT VOLTAGE OUTPUT ERROR						
QVO Ratiometry Error [2]	$V_{RatErrQVO}$	$V_{CC} = \pm 3\%$ variation of nominal supply voltage	-5	± 2	5	mV
Quiescent Voltage Output Temperature Error	$V_{OUT(Q)TC}$	$T_A = 25^\circ\text{C}$ to 150°C , up to $\pm 40\%$ of sensitivity change	-5	± 3	5	mV
		$T_A = -40^\circ\text{C}$ to 25°C , up to $\pm 40\%$ of sensitivity change	-5	± 3	5	mV
LIFETIME DRIFT CHARACTERISTICS [3]						
QVO Lifetime Drift	$V_{OUT(Q)LIFE}$	Initial sensitivity	-	± 4.7	-	mV
Sens Lifetime Drift	$Sens_{LIFE}$	Initial sensitivity	-	± 0.75	-	%
Additional QVO Temperature Error Relative to 25°C Due to Lifetime		$T_A = -40^\circ\text{C}$ to 150°C , initial sensitivity	-	1.1	-	mV
Additional Sensitivity Error Relative to 25°C Due to Lifetime		$T_A = -40^\circ\text{C}$ to 150°C , initial sensitivity	-	0.1	-	%

[1] Noise scales with sensitivity.

[2] For lower V_{CC} variations than test conditions, Ratiometry Error linearly scales with V_{CC} , e.g. $\pm 1.5\%$ variations on V_{CC} instead of $\pm 3\%$ leads to $Rat_{ErrSens}$ and $V_{RatErrQVO}$ to be divided by 2.

[3] Lifetime drift characteristics are based on the AEC-Q100 qualification results from zero-hour reads. Typical values are the worst-case observed drift, ± 3 sigma, during AEC-Q100 qualification from any of the -40°C , 25°C , or 150°C temperatures.

-020B5 PERFORMANCE CHARACTERISTICS: Valid over full range of T_A and $V_{CC} = 5\text{ V}$, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
NOMINAL PERFORMANCE						
Differential Magnetic Range	B_{DIFF}	Corresponding full-scale magnetic range based on typical sensitivity	-100	-	100	G
Initial Factory-Programmed Sensitivity	Sens	Factory-programmed sensitivity; $T_A = 25^\circ\text{C}$	19.7	20	20.3	mV/G
Initial Quiescent Output Voltage	$V_{OUT(Q)}$	Factory-programmed quiescent output voltage; $T_A = 25^\circ\text{C}$	2.4925	2.5	2.5075	V
Noise [1]	V_N	$T_A = 25^\circ\text{C}$, $C_L = 1\text{ nF}$, $BW_i = 250\text{ kHz}$, initial sensitivity	-	10	-	mV _{RMS}
Nonlinearity	E_{LIN}	Tested up to full-scale output	-0.55	± 0.25	0.55	%
SENSITIVITY ERROR						
Sens Ratiometry Error [2]	$Rat_{ErrSens}$	$V_{CC} = \pm 3\%$ variation of nominal supply voltage	-1	± 0.4	1	%
Sensitivity Drift Over Temperature	$\Delta Sens_{TC}$	$T_A = 25^\circ\text{C}$ to 150°C , initial sensitivity	-1.5	± 1	1.5	%
		$T_A = -40^\circ\text{C}$ to 25°C , initial sensitivity	-1.5	± 1	1.5	%
		$T_A = 25^\circ\text{C}$ to 150°C , $\pm 40\%$ sensitivity change	-1.6	± 1	1.6	%
		$T_A = -40^\circ\text{C}$ to 25°C , $\pm 40\%$ sensitivity change	-1.6	± 1	1.6	%
QUIESCENT VOLTAGE OUTPUT ERROR						
QVO Ratiometry Error [2]	$V_{RatErrQVO}$	$V_{CC} = \pm 3\%$ variation of nominal supply voltage	-7.5	± 3	7.5	mV
Quiescent Voltage Output Temperature Error	$V_{OUT(Q)TC}$	$T_A = 25^\circ\text{C}$ to 150°C , initial sensitivity	-10	± 4	10	mV
		$T_A = -40^\circ\text{C}$ to 25°C , initial sensitivity	-10	± 4	10	mV
		$T_A = 25^\circ\text{C}$ to 150°C , $\pm 40\%$ sensitivity change	-14	± 4	14	mV
		$T_A = -40^\circ\text{C}$ to 25°C , $\pm 40\%$ sensitivity change	-14	± 4	14	mV
LIFETIME DRIFT CHARACTERISTICS [3]						
QVO Lifetime Drift	$V_{OUT(Q)LIFE}$	Initial sensitivity	-	± 10.2	-	mV
Sens Lifetime Drift	$Sens_{LIFE}$	Initial sensitivity	-	± 1.1	-	%
Additional QVO Temperature Error Relative to 25°C Due to Lifetime		$T_A = -40^\circ\text{C}$ to 150°C , initial sensitivity	-	1	-	mV
Additional Sensitivity Error Relative to 25°C Due to Lifetime		$T_A = -40^\circ\text{C}$ to 150°C , initial sensitivity	-	0.1	-	%

[1] Noise scales with sensitivity. Tested with initial sensitivity.

[2] For lower V_{CC} variations than test conditions, Ratiometry Error linearly scales with V_{CC} . e.g. $\pm 1.5\%$ variations on V_{CC} instead of $\pm 3\%$ leads to $Rat_{ErrSens}$ and $V_{RatErrQVO}$ to be divided by 2.

[3] Lifetime drift characteristics are based on the AEC-Q100 qualification results from zero-hour reads. Typical values are the worst-case observed drift, ± 3 sigma, during AEC-Q100 qualification from any of the -40°C , 25°C , or 150°C temperatures.

-020U5 PERFORMANCE CHARACTERISTICS: Valid over full range of T_A and $V_{CC} = 5\text{ V}$, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
NOMINAL PERFORMANCE						
Differential Magnetic Range	B_{DIFF}	Corresponding full-scale magnetic range based on typical sensitivity	0	–	200	G
Initial Factory-Programmed Sensitivity	Sens	Factory-programmed sensitivity; $T_A = 25^\circ\text{C}$	19.7	20	20.3	mV/G
Initial Quiescent Output Voltage	$V_{OUT(Q)}$	Factory-programmed quiescent output voltage; $T_A = 25^\circ\text{C}$	0.49	0.5	0.51	V
Noise [1]	V_N	$T_A = 25^\circ\text{C}$, $C_L = 1\text{ nF}$, $BW_i = 250\text{ kHz}$, initial sensitivity	–	10	–	mV _{RMS}
Nonlinearity	E_{LIN}	Tested up to full-scale output	–0.75	± 0.25	0.75	%
SENSITIVITY ERROR						
Sens Ratiometry Error [2]	$Rat_{ErrSens}$	$V_{CC} = \pm 3\%$ variation of nominal supply voltage	–1	± 0.4	1	%
Sensitivity Drift Over Temperature	$\Delta Sens_{TC}$	$T_A = 25^\circ\text{C}$ to 150°C , initial sensitivity	–1.5	± 1	1.5	%
		$T_A = -40^\circ\text{C}$ to 25°C , initial sensitivity	–1.5	± 1	1.5	%
		$T_A = 25^\circ\text{C}$ to 150°C , $\pm 40\%$ sensitivity change	–1.6	± 1	1.6	%
		$T_A = -40^\circ\text{C}$ to 25°C , $\pm 40\%$ sensitivity change	–1.6	± 1	1.6	%
QUIESCENT VOLTAGE OUTPUT ERROR						
QVO Ratiometry Error [2]	$V_{RatErrQVO}$	$V_{CC} = \pm 3\%$ variation of nominal supply voltage	–10	± 3	10	mV
Quiescent Voltage Output Temperature Error	$V_{OUT(Q)TC}$	$T_A = 25^\circ\text{C}$ to 150°C , initial sensitivity	–10	± 4	10	mV
		$T_A = -40^\circ\text{C}$ to 25°C , initial sensitivity	–10	± 4	10	mV
		$T_A = 25^\circ\text{C}$ to 150°C , $\pm 40\%$ sensitivity change	–14	± 4	14	mV
		$T_A = -40^\circ\text{C}$ to 25°C , $\pm 40\%$ sensitivity change	–14	± 4	14	mV
LIFETIME DRIFT CHARACTERISTICS [3]						
QVO Lifetime Drift	$V_{OUT(Q)LIFE}$	Initial sensitivity	–	± 10.2	–	mV
Sens Lifetime Drift	$Sens_{LIFE}$	Initial sensitivity	–	± 1.1	–	%
Additional QVO Temperature Error Relative to 25°C Due to Lifetime		$T_A = -40^\circ\text{C}$ to 150°C , initial sensitivity	–	1	–	mV
Additional Sensitivity Error Relative to 25°C Due to Lifetime		$T_A = -40^\circ\text{C}$ to 150°C , initial sensitivity	–	0.1	–	%

[1] Noise scales with sensitivity.

[2] For lower V_{CC} variations than test conditions, Ratiometry Error linearly scales with V_{CC} , e.g. $\pm 1.5\%$ variations on V_{CC} instead of $\pm 3\%$ leads to $Rat_{ErrSens}$ and $V_{RatErrQVO}$ to be divided by 2.

[3] Lifetime drift characteristics are based on the AEC-Q100 qualification results from zero-hour reads. Typical values are the worst-case observed drift, ± 3 sigma, during AEC-Q100 qualification from any of the -40°C , 25°C , or 150°C temperatures.

-010B3 PERFORMANCE CHARACTERISTICS: Valid over full range of T_A and $V_{CC} = 3.3$ V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
NOMINAL PERFORMANCE						
Differential Magnetic Range	B_{DIFF}	Corresponding full-scale magnetic range based on typical sensitivity	-132	-	132	G
Initial Factory-Programmed Sensitivity	Sens	Factory-programmed sensitivity; $T_A = 25^\circ\text{C}$	9.85	10	10.15	mV/G
Initial Quiescent Output Voltage	$V_{OUT(Q)}$	Factory-programmed quiescent output voltage; $T_A = 25^\circ\text{C}$	1.645	1.65	1.655	V
Noise [1]	V_N	$T_A = 25^\circ\text{C}$, $C_L = 1$ nF, $BW_i = 250$ kHz, initial sensitivity	-	6.5	-	mV _{RMS}
Nonlinearity	E_{LIN}	Tested up to full-scale output	-0.55	± 0.15	0.55	%
SENSITIVITY ERROR						
Sens Ratiometry Error [2]	$Rat_{ErrSens}$	$V_{CC} = \pm 3\%$ variation of nominal supply voltage	-0.75	± 0.25	0.75	%
Sensitivity Drift Over Temperature	$\Delta Sens_{TC}$	$T_A = 25^\circ\text{C}$ to 150°C , up to $\pm 40\%$ of sensitivity change	-1.5	± 1	1.5	%
		$T_A = -40^\circ\text{C}$ to 25°C , up to $\pm 40\%$ of sensitivity change	-1.5	± 1	1.5	%
QUIESCENT VOLTAGE OUTPUT ERROR						
QVO Ratiometry Error [2]	$V_{RatErrQVO}$	$V_{CC} = \pm 3\%$ variation of nominal supply voltage	-10	± 2	10	mV
Quiescent Voltage Output Temperature Error	$V_{OUT(Q)TC}$	$T_A = 25^\circ\text{C}$ to 150°C , up to $\pm 40\%$ of sensitivity change	-5	± 3	5	mV
		$T_A = -40^\circ\text{C}$ to 25°C , up to $\pm 40\%$ of sensitivity change	-5	± 3	5	mV
LIFETIME DRIFT CHARACTERISTICS [3]						
QVO Lifetime Drift	$V_{OUT(Q)LIFE}$	Initial sensitivity	-	± 9.5	-	mV
Sens Lifetime Drift	$Sens_{LIFE}$	Initial sensitivity	-	± 1.4	-	%
Additional QVO Temperature Error Relative to 25°C Due to Lifetime		$T_A = -40^\circ\text{C}$ to 150°C , initial sensitivity	-	1	-	mV
Additional Sensitivity Error Relative to 25°C Due to Lifetime		$T_A = -40^\circ\text{C}$ to 150°C , initial sensitivity	-	0.1	-	%

[1] Noise scales with sensitivity. Tested with initial sensitivity.

[2] For lower V_{CC} variations than test conditions, Ratiometry Error linearly scales with V_{CC} , e.g. $\pm 1.5\%$ variations on V_{CC} instead of $\pm 3\%$ leads to $Rat_{ErrSens}$ and $V_{RatErrQVO}$ to be divided by 2.

[3] Lifetime drift characteristics are based on the AEC-Q100 qualification results from zero-hour reads. Typical values are the worst-case observed mean ± 3 sigma drift during AEC-Q100 qualification from any of the -40°C , 25°C , or 150°C temperatures.

FUNCTIONAL DESCRIPTION

Principle of Operation

When AC or DC current flows through a PCB copper trace or a busbar, as shown in Figure 8, the ACS37610 device will sense the magnetic field difference induced between its two Hall elements, HL and HR, represented by the field components BL and BR. The device output will be proportional to the differential field sensed, B_{diff} , which is proportional to the applied current. The relationship between applied current and generated field is described as:

$$B_{diff} = CF \times I,$$

where B_{diff} is the differential field (HL-HR), CF is the differential coupling factor (G/A), and I is the current through the busbar/PCB trace. As seen in this equation, the differential coupling factor (CF) is the linear relationship between the differential field sensed and the current flowing in the conductor. Different busbar shapes can be used to best answer application requirements; see application section for more details.

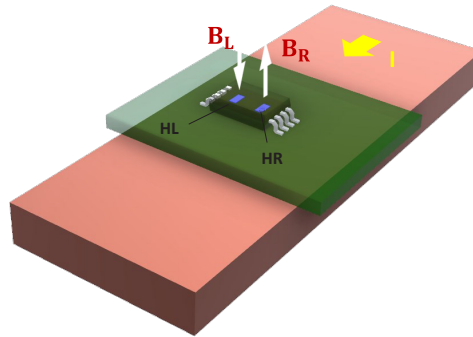


Figure 8: Current Sensing Principle

Device Diagnostics

The ACS37610 device offers multiple built-in diagnostics which effects and programmability are described in Table 1.

Table 1: Device Diagnostics Table

Diagnostic	Effect on V_{OUT}	Effect on FAULT	Note
Overvoltage detection	V_{OUT} goes high impedance if V_{CC} higher than V_{OVDE} for more than t_{OVDE} (64 μ s typ.).	FAULT goes to high-impedance state Pulled-up to V_{FAULT} .	NOTE 1: When V_{OUT} goes to high impedance state, the voltage on V_{OUT} is pulled down to GND or pulled up to V_{CC} depending on application wiring. If Com_lock bit is set, OVD feature is disabled.
Undervoltage detection	V_{OUT} pulled to GND if V_{CC} drops below V_{UVLOE} for more than t_{UVLOE} (64 μ s typ.). V_{OUT} goes high impedance if V_{CC} drops further below V_{PORL} .	FAULT goes to high-impedance state Pulled-up to V_{FAULT} .	See NOTE 1.
Broken Wire	V_{OUT} goes to high-impedance state.	FAULT goes to high-impedance state Pulled-up to V_{FAULT} .	See NOTE 1.
Overcurrent	No effect.	FAULT pin is pulled to GND.	Overcurrent threshold is programmable and can be enabled/disabled in EEPROM.
Overtemperature	No effect.	FAULT pin is pulled to GND.	Overtemperature threshold is programmable and can be enabled/disabled in EEPROM.
Clamps	V_{OUT} can range from $V_{CLP(Low)}$ to $V_{CLP(High)}$.	No effect.	Clamps can be enabled/disabled in EEPROM.
EEPROM Error Checking and Correction	If an uncorrectable error occurred in EEPROM, V_{OUT} will go to high-impedance state	FAULT goes to high-impedance state.	See NOTE 1.

Broken Wire Detection

If the GND pin is disconnected, node A becoming open (Figure 9), the VOUT pin and FAULT pin will go to a high-impedance state. The output voltage will go to $V_{BRK(HIGH)}$ if a load resistor $R_{L(PULLUP)}$ is connected to VCC or to $V_{BRK(LOW)}$ if a load resistor $R_{L(PULLDOWN)}$ is connected to GND.

If the VCC pin is disconnected, node B becoming open (Figure 9), the VOUT pin and FAULT pin will go to a high-impedance state. The output voltage will go to $V_{BRK(LOW)}$ if a load resistor

$R_{L(PULLDOWN)}$ is connected to GND.

Detection for broken VCC can only be guaranteed when a pull-down resistor is used.

Following broken wire event, the device will not respond to any applied magnetic field. If a load resistor $R_{F(PULLUP)}$ is connected to the FAULT Pin, Fault voltage will go to the $V_{F(PULLUP)}$ voltage.

If the disconnected wire is reconnected, the device will resume normal operation.

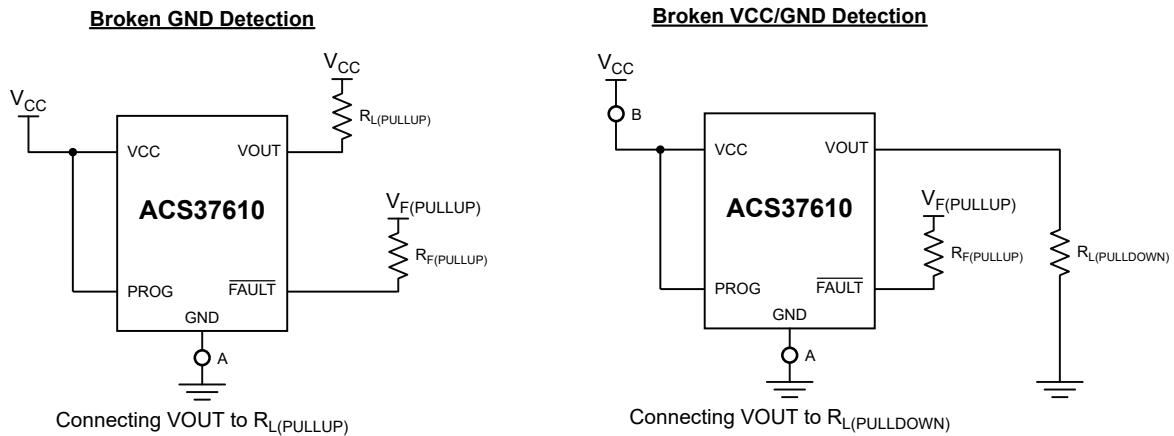


Figure 9: Connection for Detecting Broken Ground Wire

DEVICE PROGRAMMING

- The serial interface uses Manchester protocol to communicate.
- Device programming can be achieved with bidirectional communication on VOUT or on the dedicated PROG pin.
- The device has an internal charge pump to generate the EEPROM pulses.
- The Prog pin can be left unconnected or tied to GND or VCC when not used.

Serial Communication

The serial interface allows an external controller to read and write registers, including EEPROM, in the device using a point-to-point command/acknowledge protocol. The device does not initiate communication; it only responds to commands from the external controller. Each transaction consists of a command from the controller. If the command is a write, there is no acknowledging from the device. If the command is a read, the device responds by transmitting the requested data. Two modes are available for device communication.

Mode 1, Programming on VOUT pin (see Figure 10):

Voltage is raised on V_{CC} (V_{OVDE}) for at least t_{OVDE} followed by access code on VOUT to enable bidirectional programming on VOUT. If com_lock bit is set (=1), bidirectional programming on VOUT is disabled. If com_lock bit is not set (= 0), there is no timeout limit to send the access code as long as V_{CC} stays above V_{OVDE} for at least t_{OVDE}. The start of any Manchester command should begin with holding the output low for t_{BIT} to ensure reset of Manchester state machine. If an incorrect access code is sent, VOUT remains in the normal analog mode (responds to magnetic stimulus) and the device remains locked for communication on VOUT until a power reset occurs.

When writing into non-volatile memory (EEPROM), V_{CC} must not exceed 5 V to ensure safe EEPROM writing. To achieve this, two methods can be used:

Method 1 (to write EEPROM in Mode 1):

Locking VOUT into communication mode such that VCC can be returned to normal supply voltage (5 V / 3.3 V):

1. Set V_{CC} to V_{OVDE} (OVD)
2. Send Access code + comm_en
3. Set V_{CC} back to normal level (5 V / 3.3 V)
4. Send EEPROM write commands
5. Power-cycle the device to re-enable Analog output on VOUT

Method 2 (to write EEPROM in Mode 1):

Reducing V_{CC} back to normal supply voltage (5 V / 3.3 V) after sending the EEPROM write sequence:

1. Set V_{CC} to V_{OVDE} (OVD)
2. Send Access code
3. Send EEPROM write commands
4. Set V_{CC} to normal level (5 V / 3.3 V)
5. Wait 20 ms for EEPROM write

With method 2, PROG pin must not be connected to GND (can be left floating or connect to VCC).

See access code section and Manchester protocol figures for more details. When not used, it is recommended to tie PROG pin to VCC (for Broken GND feature).

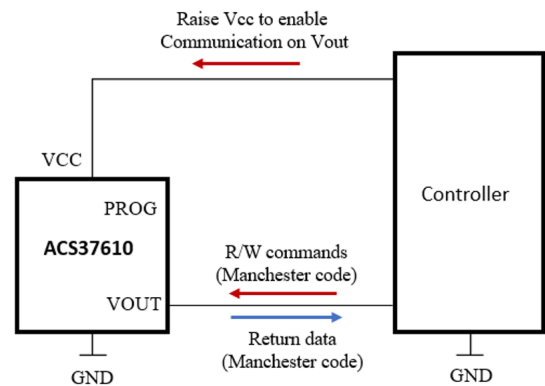


Figure 10: Programming Connection – Mode 1

Mode 2, Programming on PROG pin (see Figure 11):

V_{CC} remains 5 V (below V_{OVDE}), and bidirectional programming is achieved on PROG. Pin by sending an Access code (independently of com_lock value). No pull-up is required on PROG pin.

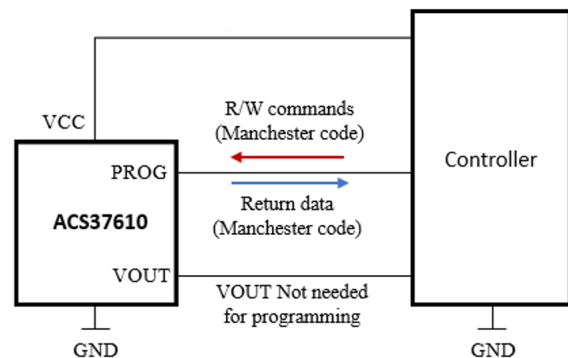


Figure 11: Programming Connections – Mode 2

Manchester Protocol

The serial interface uses a Manchester-encoding-based protocol per G.E. Thomas (0 = rising edge, 1 = falling edge), with address and data transmitted MSB first. Four commands are recognized by the device: Write Access Code, Write to Volatile Memory, Write to Non-Volatile Memory (EEPROM) and Read. One frame type, Read Acknowledge, is sent by the device in response to a Read command.

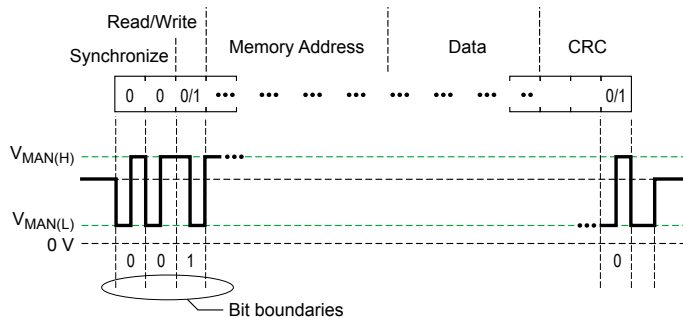


Figure 12: General Format For Serial Interface Commands

Read (Controller to Device)

The fields for the Read command are:

- Sync (2 zero bits)
- Read/Write (1 bit, must be 1 for read)
- CRC (3 bits)

Figure 13 shows the sequence for a Read command.

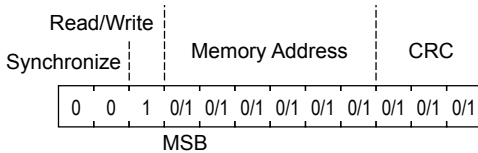


Figure 13: Read Sequence

Read Acknowledge (Device to Controller)

The fields for the data return frame are:

- Sync (2 zero bits)
- Data (32 bits):
 - [31:28] Don't Care
 - [27:26] ECC Pass/Fail
 - [25:0] Data
- CRC (3 bits)

Figure 14 shows the sequence for a Read Acknowledge. Refer to the Detecting ECC Error section for instructions on how to detect Read/Write Synchronize Memory Address Data (32 bits) and ECC failure.

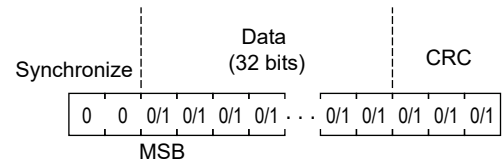


Figure 14: Read Acknowledge Sequence

Write (Controller to Device)

The fields for the Write command are:

- Sync (2 zero bits)
- Read/Write (1 bit, must be 0 for write)
- Address (6 bits)
- Data (32 bits):
 - [31:26] Don't Care
 - [25:0] Data
- CRC (3 bits)

Figure 15 shows the sequence for a Write command. Bits [31:26] are Don't Care because the device automatically generates 6 ECC bits based on the content of bits [25:0]. These ECC bits will be stored in EEPROM at locations [31:26].

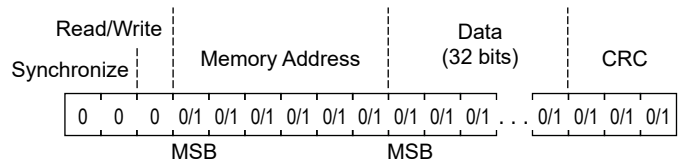


Figure 15: Write Sequence

Write Access Code (Controller to Device)

The fields for the Access Code command are:

- Sync (2 zero bits)
- Read/Write (1 bit, must be 0 for write)
- Address (6 bits)
- Data (32 bits)
- CRC (3 bits)

shows the sequence for an Access Code command.

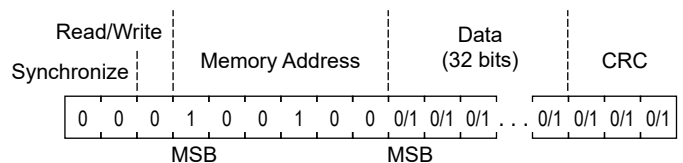


Figure 16: Write Access Code

The controller must open the serial communication with the device by sending an access code. Access code can be sent at any time on PROG pin to enable communication on PROG pin. For VOUT communication, OVD event must be sent followed by access code on VOUT. OVD event must be maintained during the first full transaction.

Register Address	Address(Hex)	Data(Hex)
Customer Access	0x31	0x2C413736
Customer Access + Com_Enable	0x31	0x2C413737

The LSB of the 32-bit customer access code is used to disable the output and leave the device in communication mode until a reset occurs. When the output is disabled, V_{CC} can be restored to a level inferior to V_{OVDE} without altering the Manchester communication and thus until a reset occurs.

Using the com_lock bit

This bit prevents VOUT from changing state following unwanted OVD event in the application. If com_lock bit is set, the OVD is disabled and the device can only be programmed using PROG pin (communication Mode 2).

Write_lock bit

Lock bit after EEPROM has been programmed by the user. The Write_lock bit can be set to 1 and VCC power-cycled to permanently disable the ability to write any EEPROM register. Volatile register can still be written to.

EEPROM Error Checking and Correction (ECC)

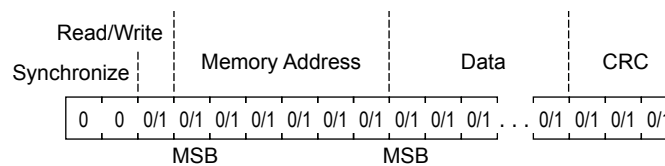
Hamming code methodology is implemented for EEPROM checking and correction. The device has ECC enabled after power-up. The device always returns 32 bits. The message received from controller is analyzed by the device EEPROM driver and ECC bits are added. The first 6 received bits from device to controller are dedicated to ECC.

The Manchester serial interface uses a 3-bit cyclic redundancy check (CRC) for data-bit error checking (synchronized bits are ignored during the check). The CRC algorithm is based on the polynomial $g(x) = x^3 + x + 1$ and is initialized to 111 when first powered up. Write commands written to the slave controller are checked against the embedded CRC field.

Detecting ECC Error

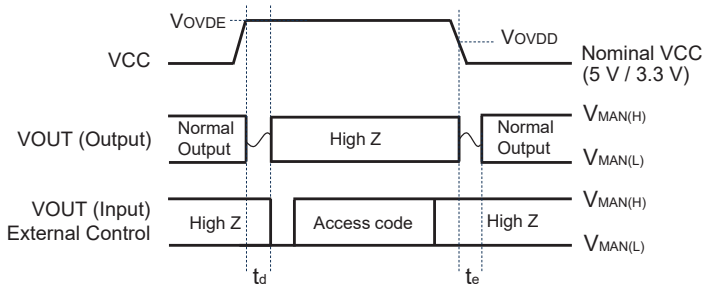
If an uncorrectable error has occurred, bits [27:26] are set to '10', the VOUT pin will go to a high-impedance state, and the device will not respond to the applied magnetic field.

Bits	Name	Description
31:28	–	No meaning
27:26	ECC	00 = No Error 01 = Error detected and message corrected 10 = Uncorrectable error 11 = No meaning
25:0	Data[25:0]	EEPROM data

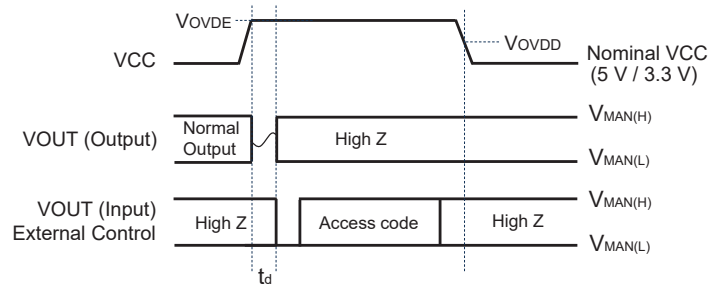


Quantity of Bits	Name	Values	Description
2	Synchronization	00	Used to identify the beginning of a serial interface command
1	Read / Write	0	[As required] Write operation
		1	[As required] Read operation
6	Address	0/1	[Read/Write] Register address (volatile memory or EEPROM)
32	Data	0/1	26 data bits and 6 ECC bits. For a read command frame the data consists of 32 bits: [31:28] Don't Care, [27:26] ECC Pass/Fail, and [25:0] Data. Where bit 0 is the LSB. For a write command frame the data consists of 32 bits: [31:26] Don't Care and [25:0] Data. Where bit 0 is the LSB.
3	CRC	0/1	Bits to check the validity of frame.

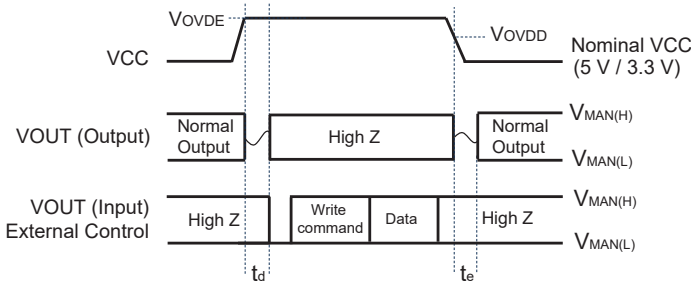
Figure 17: Command Frame General Format



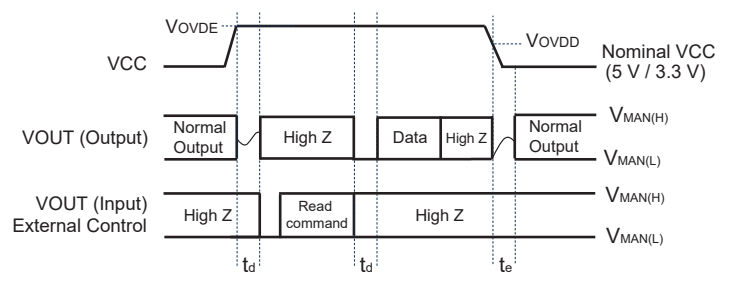
**Figure 18: VOUT programming (Mode 1)
Write Access Code**



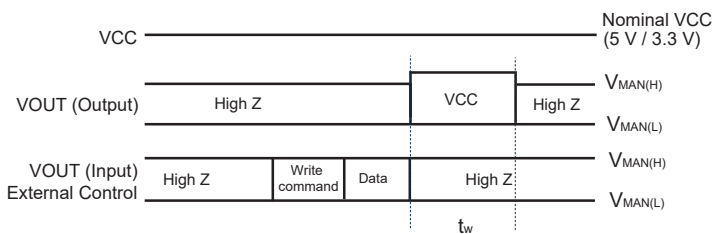
**Figure 19: VOUT programming (Mode 1)
Write Access Code + comm_en**



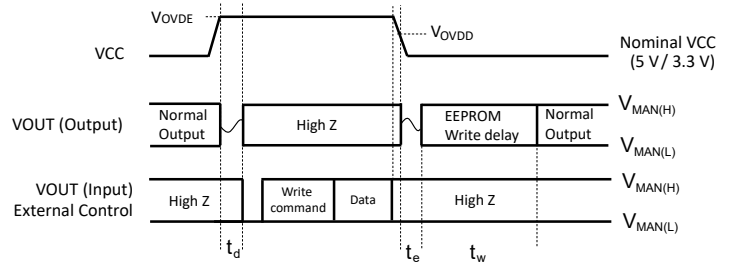
**Figure 20: VOUT programming (Mode 1)
Write Volatile Memory**



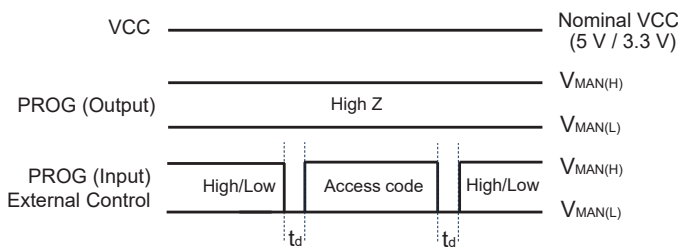
**Figure 21: VOUT programming (Mode 1)
Read Memory**



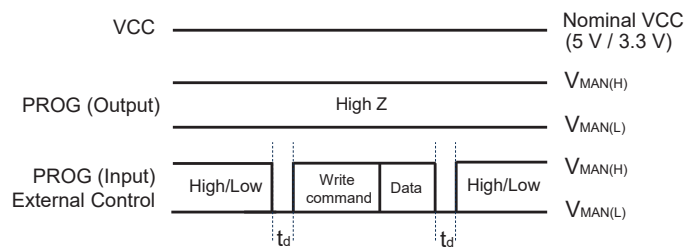
**Figure 22: VOUT programming (Mode 1)
Write to EEPROM (Method 1, comm_en = 1)**



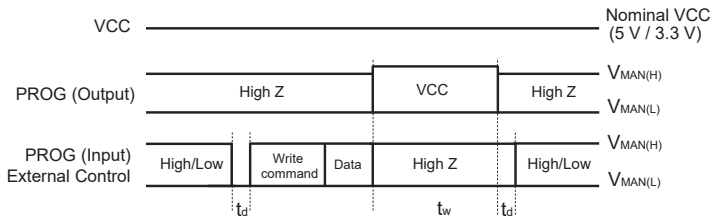
**Figure 23: VOUT programming (Mode 1)
Write to EEPROM (Method 2)**



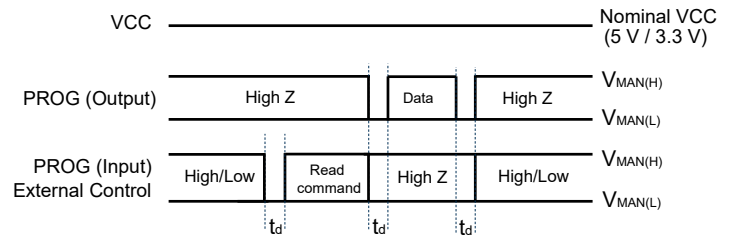
**Figure 24: PROG programming (Mode 2)
Write Access Code**



**Figure 25: PROG programming (Mode 2)
Write Volatile Memory**



**Figure 26: PROG programming (Mode 2)
Write to EEPROM**



**Figure 27: PROG Programming (Mode 2)
Read Memory**

Table 2: Programming Parameters, $C_{BYPASS} = 0.1 \mu\text{F}$, $V_{CC} = 5 \text{ V}$

Characteristics	Symbol	Note	Min.	Typ.	Max. [1]	Unit
Program Time Delay	t_d	Delay between consecutive read/writes during same Manchester event	–	74	–	μs
Program Write Delay	t_w	Delay between EEPROM writes	–	25	35	ms
Manchester High Voltage	$V_{MAN(H)}$	Data pulses on VOUT / PROG pin, $V_{CC} = 5 \text{ V}$	4	5	V_{CC}	V
		Data pulses on VOUT / PROG pin, $V_{CC} = 3.3 \text{ V}$	2.4	3.3	V_{CC}	V
Manchester Low Voltage	$V_{MAN(L)}$	Data pulses on VOUT / PROG pin, $V_{CC} = 5 \text{ V}$	0	–	1	V
		Data pulses on VOUT / PROG pin, $V_{CC} = 3.3 \text{ V}$	0	–	0.75	V
Bit Rate	t_{BITR}	Communication rate	1	30	133	kbps
Bit Time	t_{BIT}	Data bit pulse width	1000	33	7.5	μs
Output Enable Delay	t_e	External capacitance (CLX) on VOUT may increase the Output Enable Delay	–	125	–	μs

[1] Limit guaranteed by design and characterization.

EEPROM and Programming Parameters

EEPROM PROGRAMMABLE PARAMETERS: Valid through full range of T_A and V_{CC} , unless otherwise specified

Parameter	Symbol	Description	Min.	Typ. [1]	Max.	Unit	Bit	Typ. Step Size
Overcurrent Positive Fault [1]	OCF_p_thres	Programmable overcurrent/field fault positive	50	–	200	% FS	7	1.6 %
Overcurrent Negative Fault [1]	OCF_n_thres	Programmable over current/field fault negative	50	–	200	% FS	7	1.6 %
Sensitivity Fine [2]	sens_fine	Sensitivity fine adjustment; signed 2's complement	2.5	5	7.5	mV/G	9	15 μ V/G
			5	10	15	mV/G	9	30 μ V/G
			10	20	30	mV/G	9	60 μ V/G
QVO [2]	qvo	Quiescent Output Voltage adjustment ($V_{OUT(Q)}$); signed 2's complement $V_{CC} = 5$ V, bidirectional	2.4	2.5	2.6	V	9	1 mV
		Quiescent Output Voltage adjustment ($V_{OUT(Q)}$); signed 2's complement $V_{CC} = 5$ V, Unidirectional	0.4	0.5	0.6	V	9	1 mV
		Quiescent Output Voltage adjustment ($V_{OUT(Q)}$); signed 2's complement $V_{CC} = 3.3$ V, bidirectional	1.6	1.65	1.7	V	9	0.6 mV
Fault Pull-Up Disconnect	FaultR_dis	Disconnect fault pull up resistor	0	0	1	–	1	–
Polarity	Pol	Output polarity	0	0	1	–	1	–
OCF Qualifier [1]	OCF_qual	Overcurrent fault qualifier / delay, typical programmable values	0	0	12.7	μ s	3	–
Fault Latch	Fault_lat	Fault latch enable	0	0	1	–	1	–
OCF Hysteresis [1]	OCF_hyst	Overcurrent fault hysteresis, typical programmable values	11	11	75	%	2	–
OCF Disable	OCF_dis	Overcurrent fault disable	0	0	1	–	1	–
OTF Threshold [1]	OTF_thres	Overtemperature fault threshold	80	160	165	$^{\circ}$ C	4	7
OTF Fault Disabled	OTF_dis	Overtemperature fault disable	0	1	1	–	1	–
Communication Lock	Com_lock	Used to disable Manchester communication	0	0	1	–	1	–
Disabled Positive OCF Trip Point	OCF_p_dis	Disable the positive overcurrent fault trip point	0	0	1	–	1	–
Disabled Negative OCF Trip Point	OCF_n_dis	Disable the negative overcurrent fault trip point	0	0	1	–	1	–
Clamp Enable	Clamp_en	Enable clamps on the output	0	0	1	–	1	–
Customer Scratch	scratch_c	Customer scratch pad	–	–	–	–	26	–

[1] Limits guaranteed by design and characterization data, not tested in production.

[2] Although device programming range may be larger, programming sensitivity beyond +/-40% of change from initial value will cause $V_{OUT(Q)TC}$ and Δ SensTC drift to deteriorate beyond the specified values.

Lock Bits Mechanism

Device has two lock bits to disable communication and EEPROM programming. The achieved behavior is summarized Table 3 below:

Table 3: Lock Bit Mechanism

write_lock	com_lock	EEPROM Write	EEPROM Read
0	0	Yes – PROG pin or VOUT with OVD	Yes – PROG pin or VOUT with OVD
0	1	Yes – PROG pin	Yes – PROG pin
1	0	No	Yes – PROG pin or VOUT with OVD
1	1	No	Yes – PROG pin

Programming Sensitivity and Quiescent Voltage Output

Sensitivity and $V_{OUT(Q)}$ can be adjusted by programming Sens_Fine and QVO bits, as illustrated in Figure 28 and Figure 29, Sens_Fine and QVO codes use a 2's complement encoding to either reduce or increase sensitivity and $V_{OUT(Q)}$. Customers should not program sensitivity or $V_{OUT(Q)}$ beyond the maximum or minimum programming ranges specified in the Operating Characteristics table. Exceeding the specified limits will cause the sensitivity and $V_{OUT(Q)}$ drift over the temperature range (E_{Drift} and V_{OED}) to deteriorate beyond the specified values. Programming sensitivity might cause a small drift in $V_{OUT(Q)}$. As a result, it is recommended to program sensitivity first, then $V_{OUT(Q)}$.

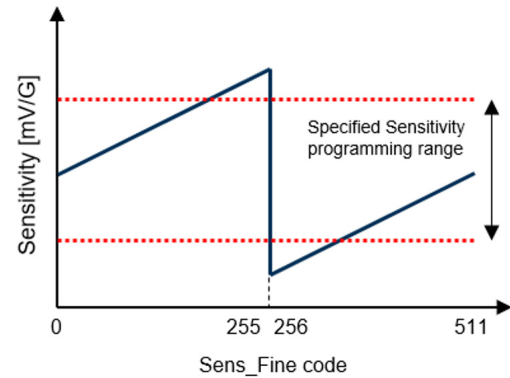


Figure 28: Sensitivity Trim Range

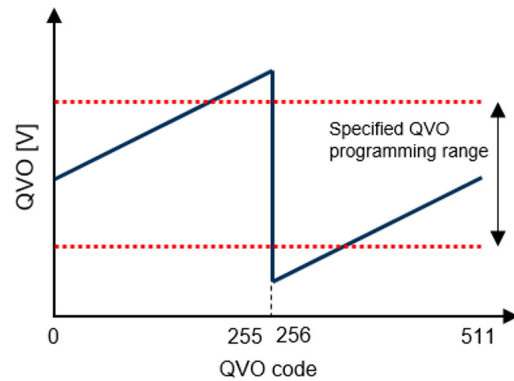


Figure 29: QVO Trim Range

Polarity “Pol”

Device output polarity is programmable to 1 (Default) or 0; this allows output polarity to be reversed. Default polarity (Pol bit set to ‘1’) corresponds to an increasing output from 2.5 to 4.5 V typical (0.5 to 4.5 V on unidirectional versions) when positive current flows from pin 1 to pin 4 (or pin 8 to pin 5) as shown in Figure 30 and Figure 31. Note that changing device polarity from its initial programmed value can cause offset error $V_{OUT(Q)TC}$ to exceed specification limits.

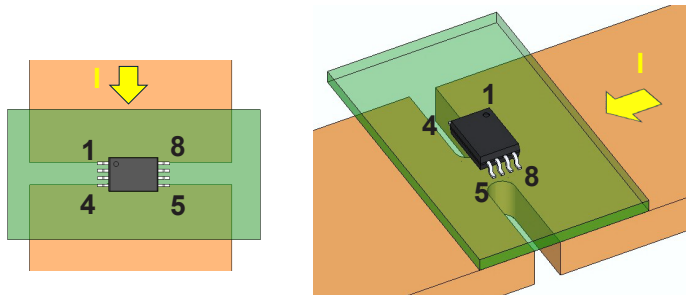


Figure 30: Polarity Definition in Planar Configuration

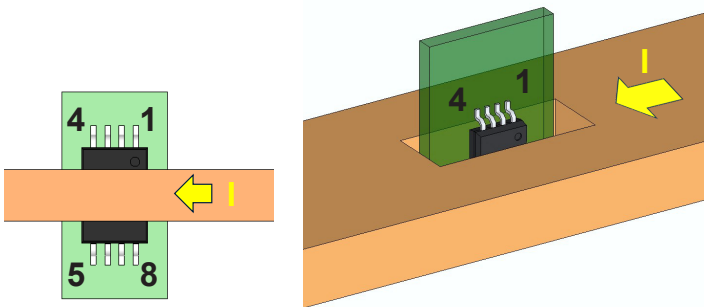


Figure 31: Polarity Definition in Vertical Configuration

Positive Overcurrent Fault Threshold

This sets the threshold for the OCF when current induces a positive output response on V_{OUT} (increasing V_{OUT} value from 2.5 to 4.5 V on 5 V bidirectional variant or 0.5 to 4.5 V for 5 V unidirectional variant); see Figure 32. Threshold can be set independently from OCF_{n_thresh} and can be disabled in device memory by setting OCF_{p_dis} to “1”

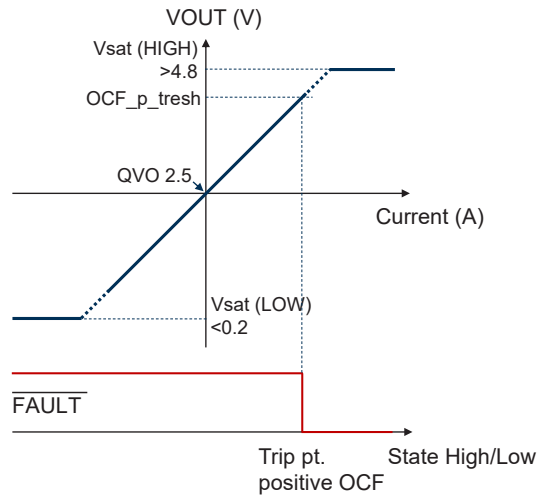


Figure 32: Positive OCF Threshold

Negative Overcurrent Fault Threshold

This sets the threshold for the OCF when current induces a negative output response on V_{OUT} (decreasing V_{OUT} value from 2.5 to 0.5 V on 5 V bidirectional variant); see Figure 33. Threshold can be set independently from OCF_{p_thresh} and can be disabled in device memory by setting OCF_{n_dis} to “1”. OCF_{n_thresh} feature is only usable in bidirectional variant.

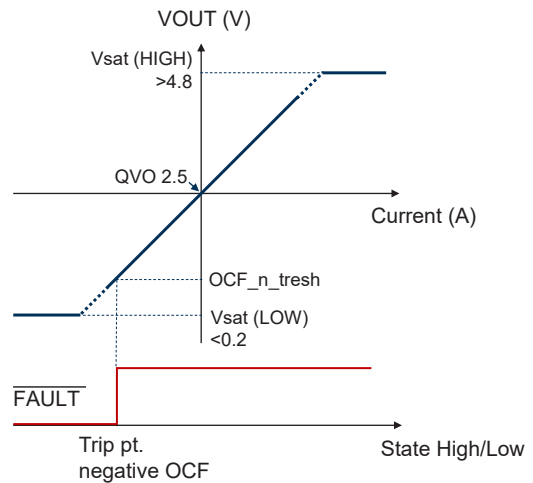


Figure 33: Negative OCF threshold

Fault Latch “Fault_latch”

When Fault latch bit is set to “1”, the device needs to be power-cycled to release the Fault condition (following an overcurrent or overtemperature event). By default, this is set to “0” (disabled).

When Fault_latch is disabled, the device relies on the programmed hysteresis value to release the Fault.

Figure 34 shows Fault output behavior following an overcurrent condition. When Fault_latch bit set to “1”, Fault remains activated (Low state) until the device is power-cycled.

Figure 35 shows Fault output behavior following an overcurrent condition. When Fault_latch bit set to “0”, the Fault will be release once the current is reduced below the overcurrent threshold hysteresis level (OCF_p_thresh minus OCF_hyst for positive OCF threshold and OCF_n_thresh minus OCF_hyst for negative OCF threshold).

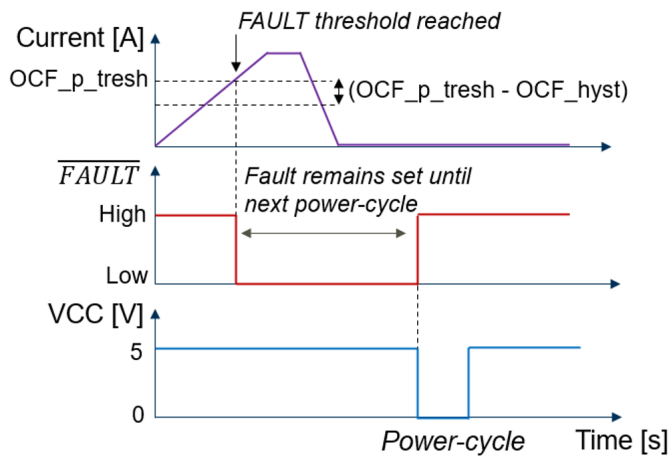


Figure 34: Fault Behavior with “Fault Latch = 1”

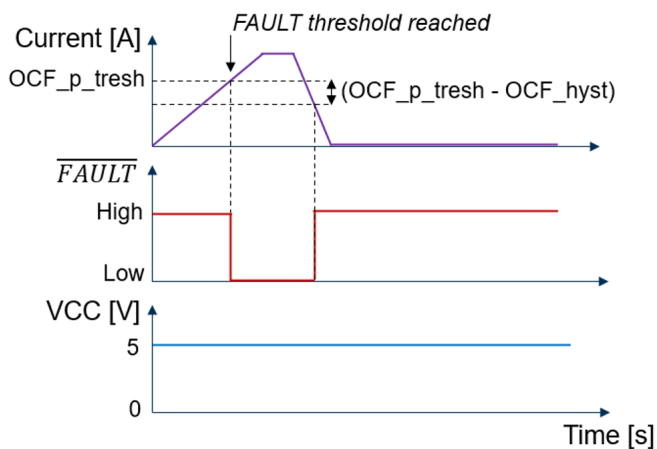


Figure 35: Fault Behavior with “Fault Latch = 0”

Overcurrent Fault Qualifier “OCF_Qual”

Overcurrent Fault qualifier sets the amount of time the overcurrent condition must be detected before triggering the Fault output. This acts as a filter on the fault condition to prevent incorrect triggering of the Fault output in case of quick current spikes or ripples.

Overcurrent must be above the specified threshold for the duration of the Fault Qualifier (OCF_Qual) in order to be flagged, as seen in example Figure 36 and Figure 37.

This delay does not apply to the condition for releasing the fault, once hysteresis condition is fulfilled, the Fault is released after $t_{C(F)}$.

OCF_qual range is described in Table 4 below.

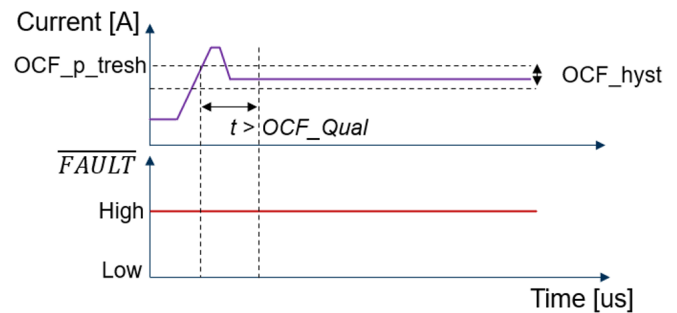


Figure 36: Fault not triggered if current is above OCF threshold for less than OCF_Qual

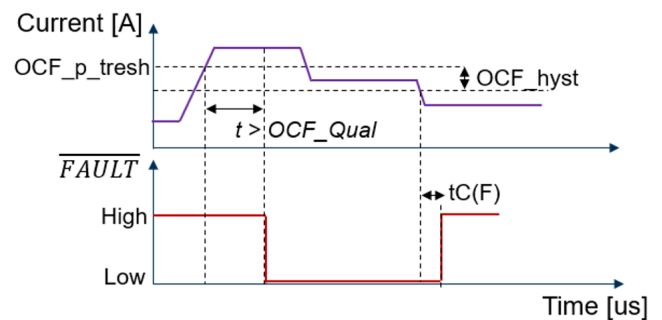


Figure 37: Fault triggered when current is above OCF threshold for more than OCF_Qual, the Fault is then released when current is below hysteresis

Table 4: Overcurrent Fault Qualifier

Setting	Typ. Delay to Fault	Units
0	2.3	μs
1	2.9	μs
2	5	μs
3	7.6	μs
4	10.1	μs
5	12.6	μs
6	15.3	μs
7	17.9	μs

Overcurrent Fault Hysteresis “Ocf_hyst”

This sets the hysteresis value applied to the OCF threshold such that once triggered the current must return below the hysteresis level to release the Fault output. This feature prevents chattering of the Fault pin due to noise.

Figure 38 shows hysteresis principle, e.g : OCF_p_tresh = 110% with Ocf_hyst = 12.5% corresponds to a fault trip point at 110% (2.2 V output sweep if V_{CC} = 5 V) and a release point at 97.5% (2.2 V output sweep if V_{CC} = 5 V).

Programming values of OCF_Hyst are shown Table 5.

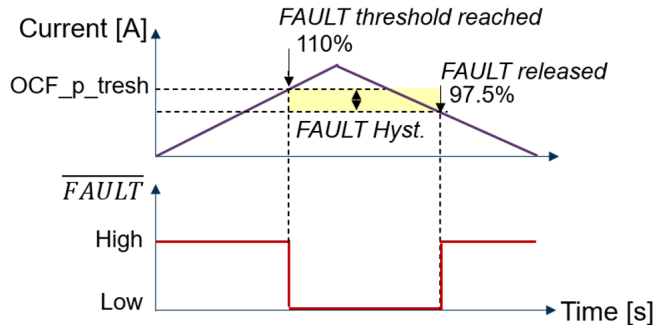


Figure 38: Hysteresis effect on Fault

Table 5: Overcurrent Fault Hysteresis

Setting	Typ. Value [1]	Units
0	11	%
1	22	%
2	42	%
3	75	%

[1] Hysteresis value cannot be greater than the minimum OCF threshold specified minus 25%, e.g. If OCF_p is set at 50%, the maximum hysteresis value will be 50-25 = 25%, such that OCF_hyst = 2 or 3 will result to a maximum hysteresis value of 25%.

Temperature Output “Temp_Out”

This feature allows to read the device temperature stored into a 12-bit digital value.

Formula below can be used to convert digital temperature to ambient temperature in degree Celsius.

$$\text{TempAmbient } [^{\circ}\text{C}] = (\text{Temp_Out} - 2200) / 13.5 + 25$$

Note: Due to device self-heating the temperature reaches 90% of its steady state after approximately 10 seconds after power-on.

Temperature accuracy is indicated in “FAULT CHARACTERISTICS” table and is guaranteed by characterization only.

MEMORY MAP

Register Name	Address	Parameter Name	Description	Access	Size	MSB	LSB
EEPROM: (ee_cust0) Shadow register [1]: (sh_cust0)	EEPROM: (0x09) Shadow register [1]: (0x19)	Write_lock	Lock the device	R/W	1	25	25
		Com_lock	Disables communication on VOUT / disables OVD	R/W	1	24	24
		Spare	n/a	R/W	1	23	23
		OTF_dis	Disable overtemperature fault	R/W	1	22	22
		Pol	Change output polarity	R/W	1	21	21
		Clamp_en	Enable output clamps	R/W	1	20	20
		Fault_dis	Disable fault	R/W	1	19	19
		FaultPup_dis	Disconnect fault internal pull-up resistor	R/W	1	18	18
		Qvo	Offset adjustment	R/W	9	17	9
		Sns_fine	Sensitivity fine adjustment	R/W	9	8	0
EEPROM: (ee_cust1) Shadow register [1]: (sh_cust1)	EEPROM: (0x0A) Shadow register [1]: (0x1a)	OCF_hyst	Overcurrent fault hysteresis	R/W	2	25	24
		Fault_latch	Enable fault latch	R/W	1	23	23
		OCF_p_dis	Disable positive overcurrent fault	R/W	1	22	22
		OCF_n_dis	Disable negative overcurrent fault	R/W	1	21	21
		OCF_qualifier	Overcurrent fault qualifier / short pulse filter	R/W	3	20	18
		OTF_thresh	Overtemperature fault threshold	R/W	4	17	14
		OCF_n_thres	Negative overcurrent fault threshold	R/W	7	13	7
OCF_p_thres	Positive overcurrent fault threshold	R/W	7	6	0		
EEPROM: (ee_cust2)	EEPROM: (0x0B)	C_spare	Customer scratchpad No effect on device functionality	R/W	26	25	0
Volatile register: (fault_status)	Volatile register: (0x20)	Temp_out	Temperature output	R	12	27	16
		uv_stat	Undervoltage status	R	1	12	12
		ov_stat	Overvoltage status	R	1	11	11
		oc_stat	Overcurrent status	R	1	10	10
		ot_stat	Overtemperature status	R	1	9	9
		fp_stat	FAULT pin status	R	1	8	8
		uv_ev	Undervoltage event	R	1	4	4
		ov_ev	Overvoltage event	R	1	3	3
		oc_ev	Overcurrent event	R	1	2	2
		ot_ev	Overtemperature event	R	1	1	1
		fp_ev	FAULT pin event	R	1	0	0

[1] Shadow registers are volatile memory, upon startup device loads EEPROM memory into shadow registers. Shadow registers can be used to test different programming options without erasing EEPROM (e.g finding sensitivity and QVO codes before writing into EEPROM).

DEFINITIONS OF ACCURACY CHARACTERISTICS

SENSITIVITY (Sens)

The amount of the output voltage increase is proportional to the magnitude of the magnetic field applied. This proportionality is specified as the magnetic sensitivity, Sens (mV/G), of the device, and it is defined as:

$$Sens = \frac{V_{OUT(B1)} - V_{OUT(B2)}}{B1 - B2}$$

where B1 and B2 are two different magnetic field levels.

SENSITIVITY ERROR

The sensitivity error is the percent difference between the measured sensitivity and the ideal sensitivity. For example, in the case of $V_{CC} = 5\text{ V}$:

$$E_{Sens} = \frac{Sens_{Meas(5V)} - Sens_{Ideal(5V)}}{Sens_{Ideal(5V)}} \times 100\%$$

SENSITIVITY ERROR RELATIVE TO SENSITIVITY AT 25°C ($\Delta SENS_{TC}$)

The Sensitivity Error Relative to Sensitivity at 25°C is the percent difference between the measured sensitivity at a given temperature and the sensitivity measured at 25°C. For example, in the case of $V_{CC} = 5\text{ V}$:

$$\Delta SENS_{TC} = \frac{Sens_{Meas(5V)} - Sens_{Meas25C(5V)}}{Sens_{Meas25C(5V)}} \times 100\%$$

NONLINEARITY (E_{LIN})

Nonlinearity is a measure of how linear the output of the sensor IC is over the full current measurement range. The nonlinearity is calculated as:

$$E_{LIN} = \left\{ 1 - \left[\frac{Sens_{BPRMax}}{Sens_{BPRHalf}} \right] \right\} \times 100\%$$

where $Sens_{BPRMax}$ is the sensitivity measured at the full range output level and $Sens_{BPRHalf}$ is the sensitivity measured at half of the full range output level.

RATIOMETRY

The device features a ratiometric output. This means that the quiescent voltage output, $V_{OUT(Q)}$, and the magnetic sensitivity, Sens, are proportional to the supply voltage, V_{CC} . The ratiometric change in the quiescent voltage output is defined as:

$$V_{RatERRQVO} = \left[\left(V_{OUTQ(5V)} \times \frac{V_{CC}}{5\text{ V}} \right) - V_{OUTQ(VCC)} \right] \times 1000\text{ (mV)}$$

and the ratiometric change (%) in sensitivity is defined as:

$$Rat_{ERRSens} = \left[1 - \frac{\left(\frac{Sens_{(VCC)}}{Sens_{(5V)}} \right)}{\left(\frac{V_{CC}}{5\text{ V}} \right)} \right] \times 100\%$$

and the ratiometric change (%) in clamp voltage is defined as:

$$Rat_{ERRCLP} = \left[1 - \frac{\left(\frac{V_{CLP(VCC)}}{V_{CLP(5V)}} \right)}{\left(\frac{V_{CC}}{5\text{ V}} \right)} \right] \times 100\%$$

QUIESCENT OUTPUT VOLTAGE – QVO (ZERO FIELD OUTPUT VOLTAGE)

The output of the sensor when the sensed differential field is zero (in typical applications when no current is flowing in the bus-bar/PCB). It nominally remains at $0.5 \times V_{CC}$ for a bidirectional device and $0.1 \times V_{CC}$ for a unidirectional device. For example, in the case of a bidirectional output device, $V_{CC} = 5\text{ V}$ translates into $V_{OUT(Q)} = 2.5\text{ V}$. Variation in $V_{OUT(Q)}$ can be attributed to the resolution of the Allegro linear IC quiescent voltage trim and thermal drift.

POWER-ON RESET VOLTAGE (V_{POR})

On power-up, to initialize to a known state and avoid current spikes, the device is held in Reset state. The Reset signal is disabled when V_{CC} reaches V_{PORH} and time t_{PORR} has elapsed, allowing the output voltage to go from a high-impedance state into normal operation. After t_{PORR} , the output will remain high impedance until V_{CC} exceeds V_{UVLOD} for more than t_{UVLOD} . During power-down, the Reset signal is enabled when V_{CC} reaches V_{PORL} , causing the output voltage to go into a high-impedance state.

POWER-ON RESET RELEASE TIME (t_{PORR})

When V_{CC} rises to V_{PORH} , the Power-On Reset Counter starts. The device output voltage will transition from a high-impedance state to normal operation only when the Power-On Reset Counter has reached t_{PORR} and V_{CC} has been maintained above V_{PORH} .

OVERVOLTAGE DETECTION (V_{OVD})

When V_{CC} is raised above the Overvoltage Detection enable voltage (V_{OVDE}), the ACS37610 output stage enters high impedance. V_{OUT} will float to V_{CC} with a pull-up R_L or to GND with a pull-down R_L when (V_{OVDE}) is reached. When programming the ACS37610 using V_{OUT} (Mode 1), Overvoltage Detection must be active for communication. The device output will resume normal operation after V_{CC} is below the Overvoltage Detection disable voltage (V_{OVDD}).

If the Com_lock bit is set, Overvoltage detection will be disabled and the device output will not react to overvoltage condition.

Note that Supply Voltage limits still apply for operating charac-

teristic. Following an overvoltage condition, the supply voltage should not exceed 7.5 V for more than 1 minute. See Overvoltage section for more details.

OUTPUT SATURATION VOLTAGE (V_{SAT})

When output voltage clamps are disabled, the output voltage can swing to a maximum of $V_{SAT(HIGH)}$ and to a minimum of $V_{SAT(LOW)}$.

BROKEN WIRE VOLTAGE (V_{BRK})

If the GND pin is disconnected (broken wire event), output voltage will go to $V_{BRK(HIGH)}$ (if a load resistor is connected to VCC) or to $V_{BRK(LOW)}$ (if a load resistor is connected to GND).

UNDERVOLTAGE DETECTION (V_{UVLO})

When V_{CC} drops below the Undervoltage Detection enable voltage (V_{UVLOE}), the ACS37610 output stage drops close to GND beyond the clamp or saturation voltage. The device output will resume normal operation after V_{CC} is above the Undervoltage Detection disable voltage (V_{UVLOD}).

Undervoltage detection is only active on the 5 V variant.

See Undervoltage section for more details.

LOW-POWER MODE

Device is available in low-power mode variant where the current draw by the IC is reduced through factory programming. In this variant, the output noise is increased by ~30% compared to the normal power mode variant.

DEFINITIONS OF DYNAMIC RESPONSE CHARACTERISTICS

Power-On Time (t_{PO}). When the supply is ramped to its operating voltage, the device requires a finite time to power its internal components before responding to an input magnetic field. Power-On Time, t_{PO} , is defined as the time it takes for the output voltage to settle within $\pm 10\%$ of its steady-state value under an applied magnetic field, after the power supply has reached its minimum specified operating voltage, $V_{CC(min)}$, as shown in Figure 39.

Temperature Compensation Power-On Time (t_{TC}). After Power-On Time (t_{PO}) elapses, t_{TC} is also required before a valid temperature compensated output.

Response Time ($t_{RESPONSE}$). The time interval between a) when the sensed current reaches 90% of its final value, and b) when the sensor output reaches 90% of its full-scale value, as shown in Figure 41.

Rise Time (t_r). The time interval between a) when the sensor reaches 10% of its full-scale value, and b) when it reaches 90% of its full-scale value, as shown in Figure 40.

Propagation Delay (t_{pd}). The time interval between a) when the sensed current reaches 20% of its full-scale value, and b) when the sensor output reaches 20% of its full-scale value, as shown in Figure 40.

Delay to Clamp (t_{CLP}). A large magnetic input step may cause the clamp to overshoot its steady-state value. The Delay to Clamp, t_{CLP} , is defined as: the time it takes for the output voltage to settle within $\pm 1\%$ of Clamp Voltage Dynamic Range, after initially passing through its steady-state voltage, as shown in Figure 42.

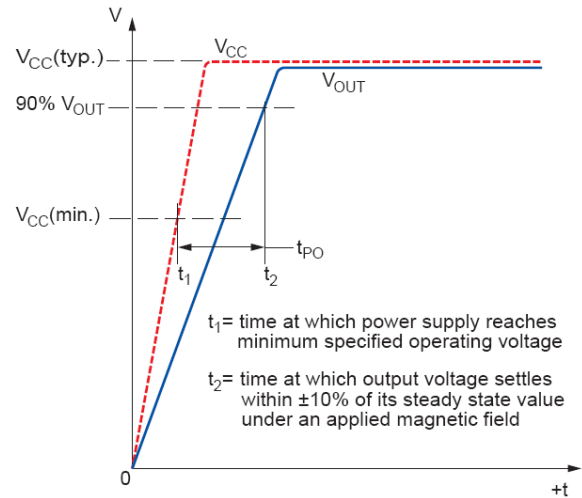


Figure 39: Power-On Time (t_{PO})

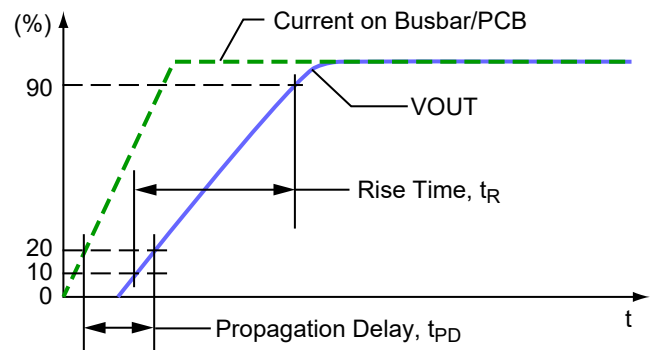


Figure 40: Propagation Delay (t_{PD}) and Rise Time (t_r)

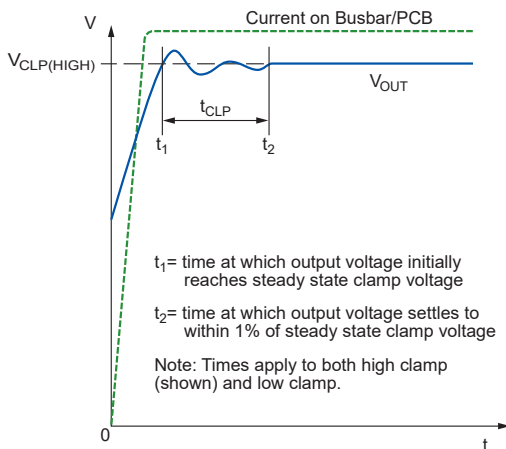


Figure 42: Delay to Clamp

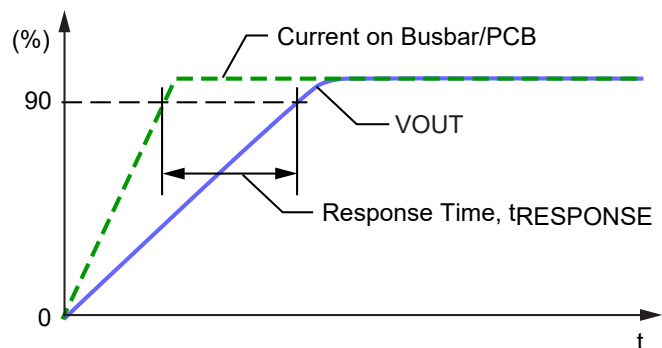


Figure 41: Response Time ($t_{RESPONSE}$)

POWER-ON RESET, UNDERVOLTAGE AND OVERVOLTAGE DETECTION OPERATION

The descriptions in this section assume: temperature = 25°C, no output load (R_L , C_L), and no significant magnetic field is present.

Power-Up. At power-up, as V_{CC} ramps up, the output is in a high-impedance state. When V_{CC} crosses V_{PORH} (location [1] in Figure 43 and [1'] in Figure 44), the POR Release counter starts counting for t_{PORR} . At this point, if V_{CC} exceeds V_{UVLOD} [2'], the output will go to $V_{CC}/2$ after t_{UVLOD} [3'].

If V_{CC} does not exceed V_{UVLOD} [2], the output will stay in the high-impedance state until V_{CC} reaches V_{UVLOD} [3] and then will go to $V_{CC}/2$ after t_{UVLOD} [4].

V_{CC} drops below $V_{CC}(min) = 4.5 V$. If V_{CC} drops below V_{UVLOE} [4', 5], the UVLO Enable Counter starts counting. If V_{CC} is still below V_{UVLOE} when counter reaches t_{UVLOE} , the UVLO function will be enabled and the output will be pulled near GND [6]. If V_{CC} exceeds V_{UVLOE} before the UVLO Enable Counter reaches t_{UVLOE} [5'], the output will continue to be $V_{CC}/2$.

Coming out of UVLO. While UVLO is enabled [6], if V_{CC} exceeds V_{UVLOD} [7], UVLO will be disabled after t_{UVLOD} , and the output will be $V_{CC}/2$ [8].

Power-Down. As V_{CC} ramps down below V_{UVLOE} [6', 9], the UVLO Enable Counter will start counting. If V_{CC} is higher than V_{PORL} when the counter reaches t_{UVLOE} , the UVLO function will be enabled and the output will be pulled near GND [10]. The output will enter a high-impedance state as V_{CC} goes below V_{PORL} [11]. If V_{CC} falls below V_{PORL} before the UVLO Enable Counter reaches t_{UVLOE} , the output will transition directly into a high-impedance state [7'].

Overvoltage. If V_{CC} goes up above V_{OVDE} , the OVD Enable Counter starts counting. If internal pullup mode is used the Fault pullup voltage will follow V_{CC} , otherwise it will remain at V_F level. If V_{CC} is still above V_{OVDE} when the counter reaches t_{OVDE} , the OVD function will be enabled and the output will go into high impedance state. Fault pin will be disabled going to high-impedance state.

Coming Out of OVD. While OVD is enabled, if V_{CC} drops below V_{OVDD} , OVD will be disabled after t_{OVDD} , and the output will return to normal operation in analog mode $V_{CC}/2$. Fault pin will become active and recover normal operation.

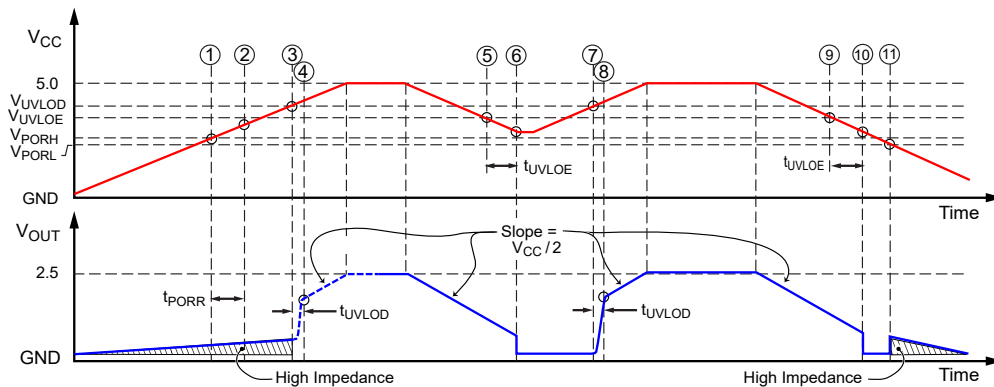


Figure 43: POR and UVLO Operation – Slow Rise Time Case – 5 V Variant

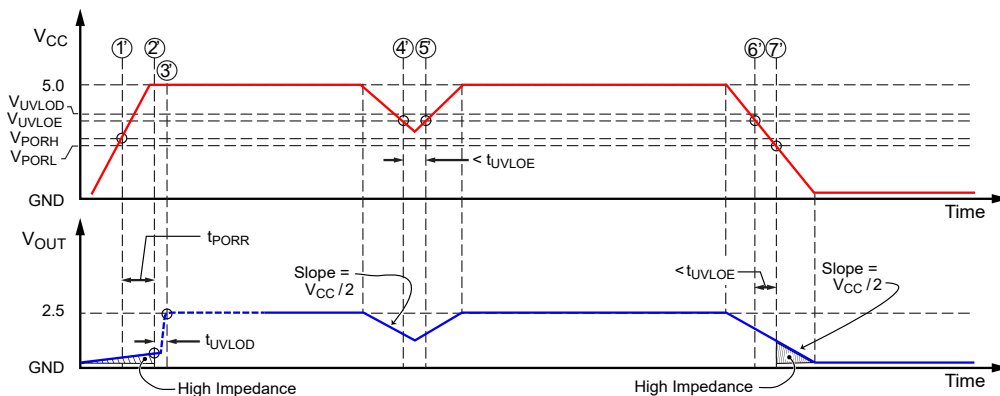


Figure 44: POR and UVLO Operation – Fast Rise Time Case – 5 V Variant

Power-On Reset (POR); Undervoltage Lockout (UVLO) Disabled – Nominal Supply Voltage = 3.3 V

Power-Up

At power-up, as V_{CC} ramps up, the output is in a high-impedance state. When V_{CC} crosses V_{PORH} (location [1] in Figure 45 and [1'] in Figure 46), the POR Release counter starts counting for t_{PORR} [2], [2'] and the output will go to $V_{CC} / 2$ after t_{PORD} [3], [3']. The temperature compensation engine will then adjust the device Sensitivity and QVO after time t_{TC} [4], [4'].

V_{CC} drops below $V_{CC}(\min) = 3 V$

If V_{CC} drops below V_{PORH} [5'] but remains higher than V_{PORL} [6'], the output will continue to be $V_{CC} / 2$.

Power-Down

As V_{CC} ramps down below V_{PORL} [5],[7'], the output will enter a high-impedance state.

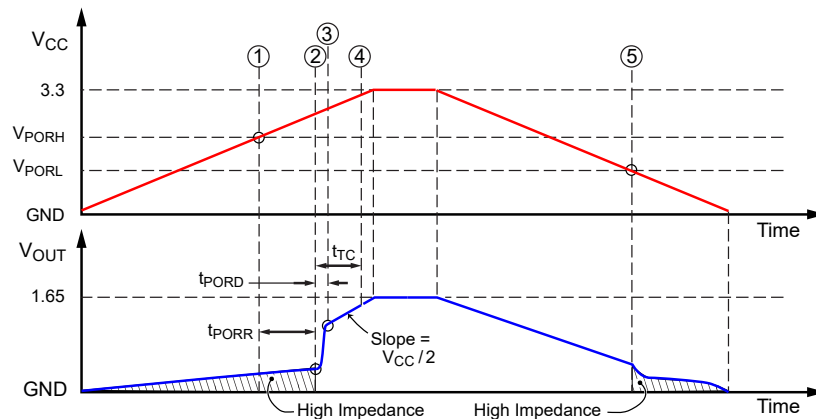


Figure 45: POR and UVLO Operation – Slow Rise Time Case – 3.3 V Mode

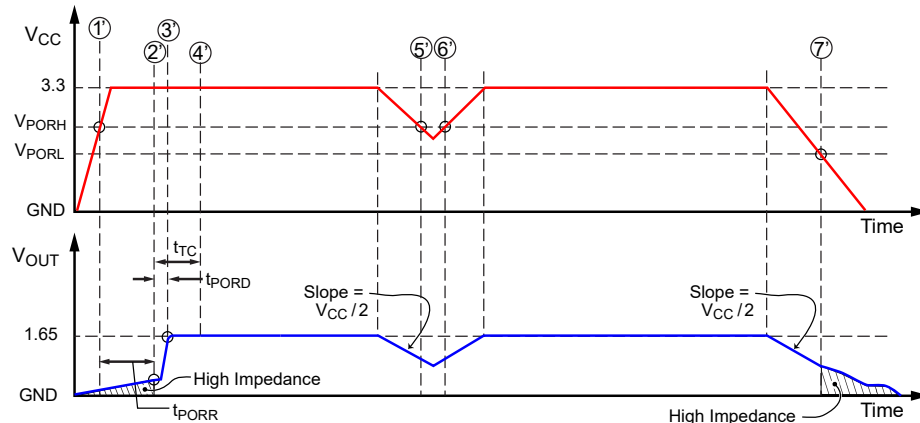


Figure 46: POR and UVLO Operation – Fast Rise Time Case – 3.3 V Mode

APPLICATION INFORMATION

Typical Application – Busbar Current Sensing

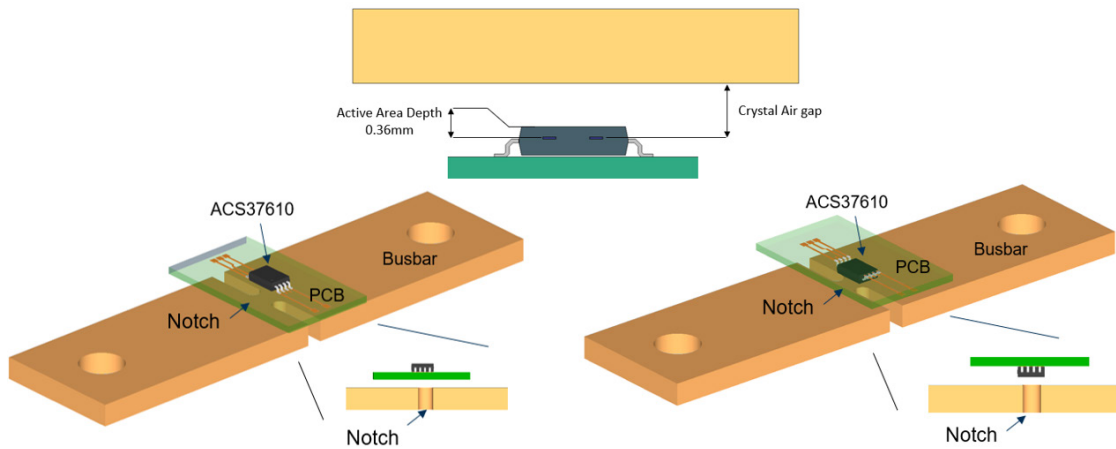


Figure 47: Busbar current sensing application – reference busbar design with notch

The ACS37610 is ideal for busbar current sensing applications. For a given current flowing through the busbar, the magnitude of the differential magnetic field sensed by the IC will depend on the air gap between the busbar and the IC. Adding a notch (width reduction) to the busbar at the location where the sensor is placed significantly increases the magnitude of the magnetic field, improving SNR.

Keeping the notch length short (2 to 3 mm) results in virtually no increase in the resistance of the busbar or degradation of its thermal performance.

Different busbar and notch dimensions can be used to optimize system performance and respond to application constraints. Figure 47 and Table 6 highlight the dimensions of an Allegro evaluation board designed to measure ± 1000 A.

Note: Comparing the busbar described in Figure 47 to a bare busbar (without notch), the busbar with the 3 mm notch increased the overall impedance by less than $10 \mu\Omega$, increasing busbar temperature by only few degrees during testing.

Skin Effect Consideration

Skin effect in the conductor tends to reduce the magnitude of the differential magnetic field measured by the IC at high frequencies (coupling factor) and therefore will influence the bandwidth of the system and response time to transient current.

Skin effect will depend on busbar dimensions, sensor mounting orientation, and distance between the busbar and the IC. A short notch width (~ 3 mm) and a busbar thickness of 4 mm will provide the best response over frequency.

Table 6: Current range based on reference busbar design:

Busbar Application	Cross Section [mm ²]	Notch Cross Section [mm ²]	Max. Current [2] [A]	Coupling Factor [1] [G/A]	Diff. Field [1] [G]	IC Sensitivity [1] [mV/G]
16 × 4 mm Busbar + 4.5 mm Notch	64	18	± 1100	0.17	± 200	10

[1] Considering a distance from hall elements to busbar of 3 mm.

[2] Full-scale current is required to cover the full-scale output range (bidirectional = ± 2 V).

Multiple Busbar Design Options

The ACS37610 offers many different mounting possibilities, addressing different needs (bandwidth, mounting tolerances, and crosstalk). The figures below show different mounting options.

Refer to Allegro's website (<https://www.allegromicro.com>) for application notes explaining the tradeoffs between different topologies.

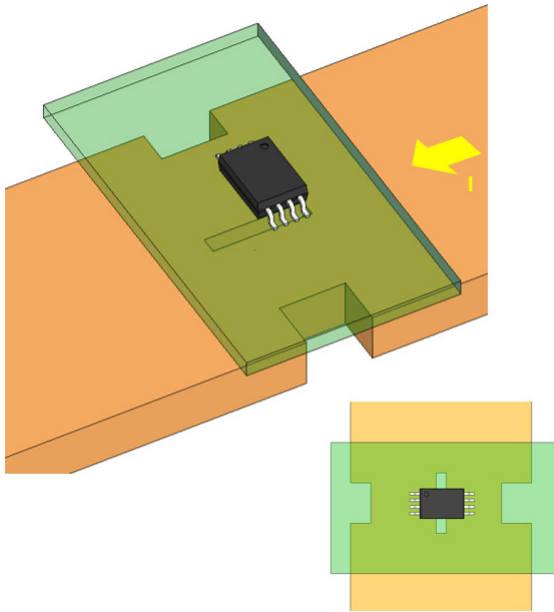


Figure 48: Rift Busbar Design

High mounting tolerances, medium coupling factor, high skin effect.
For DC to low frequency AC applications <1 kHz.

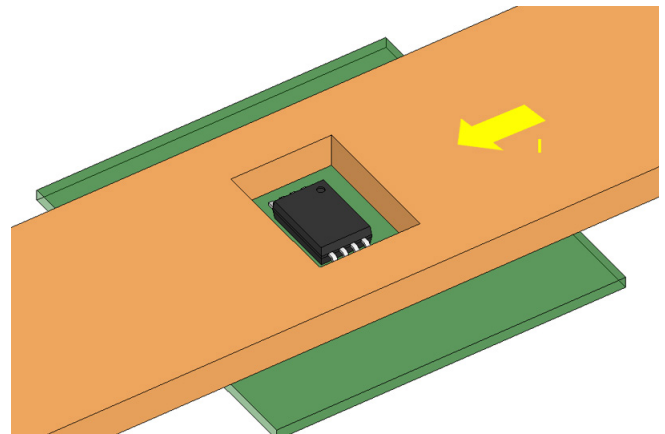


Figure 49: Slit Busbar Design

High mounting tolerances, medium coupling factor, medium skin effect.
For DC to medium frequency AC applications <100 kHz.

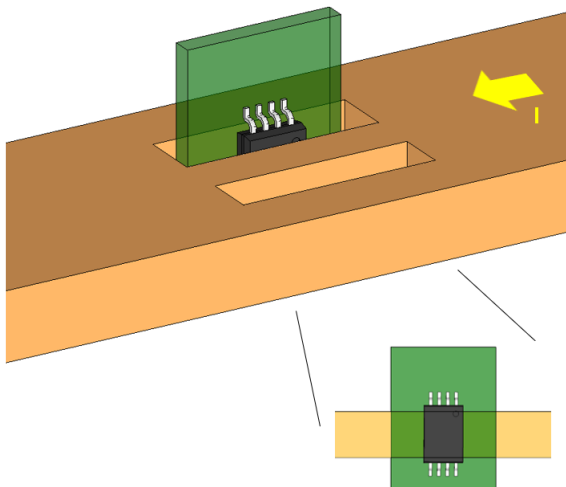


Figure 50: Dual Vertical Slit Busbar Design

High mounting tolerances, high coupling factor, low skin effect.
For DC to high frequency AC applications >100 kHz.

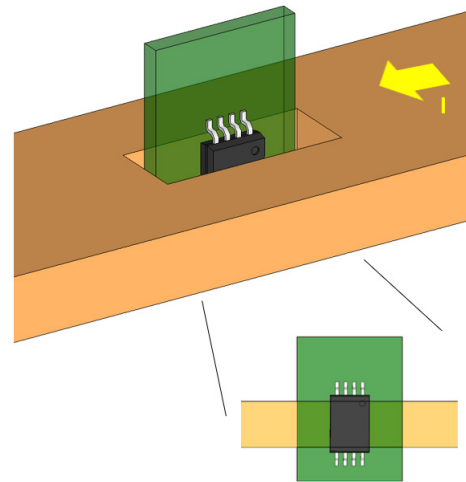


Figure 51: Vertical Slit Busbar Design

High mounting tolerances, high coupling factor, low skin effect.
For DC to high frequency AC applications >100 kHz.

Typical Application – PCB Sensing

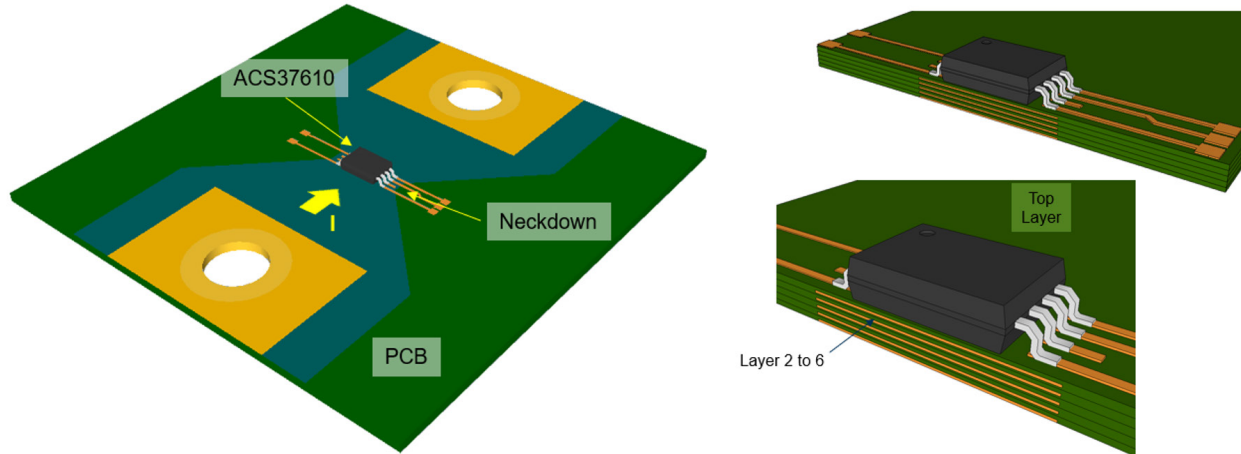


Figure 52: PCB Current sensing application – 6-Layer reference PCB example

The ACS37610 can also be used in PCB applications where the current flows directly in the PCB instead of on a busbar.

Multiple copper layers can be used to carry the current. Reducing the width of the copper traces under the sensor (neckdown) increases the magnitude of the differential magnetic field measured by the IC.

Different copper layer dimensions and stackups can be used to optimize performance and are specific to the constraints of the application. For example, in higher voltage applications, the top layer would only be used for signal routing in order to use the PCB replaced by dielectric layer for isolation.

Figure 52 and Table 7 highlight the dimensions of three Allegro evaluation boards designed to measure a wide current range.

Care must be taken when routing the device signal to prevent

noise coupling to the supply or output lines.

The power plane in the neckdown area should also be avoided to prevent disturbing the magnetic field measured.

Skin Effect Consideration

Skin effect in the PCB current-carrying traces will tend to reduce the differential magnetic field measured by the IC at high frequencies (coupling factor) and therefore will influence the bandwidth of the system and response time to transient current.

Skin effect is generally limited on PCB application due to thin copper layer thickness, but the effect will depend on PCB copper trace dimensions, number of layers, and layer thickness.

Skin effect will depend on PCB copper trace dimensions, number of layers, and layer thickness.

Table 7: Current range based on reference PCB design:

PCB Application [1]	Maximum Current (A) [2]	Coupling Factor (G/A) [1]	Differential Field (G) [1]	IC Sensitivity (mV/G) [1]
8 Layers – Ref designs [3]	±100	0.9	±90	22.2
	±200	0.9	±180	11.1

[1] Typical values, not including device placement and PCB manufacturing tolerances.

[2] Full-scale current required to cover the full-scale output range (bidirectional = ±2 V).

[3] Maximum continuous current without proper cooling on this Allegro evaluation PCB design should not exceed 150 A.

PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000381, Rev. 1 and JEDEC MO-153AA)

NOT TO SCALE

Dimensions in millimeters

Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

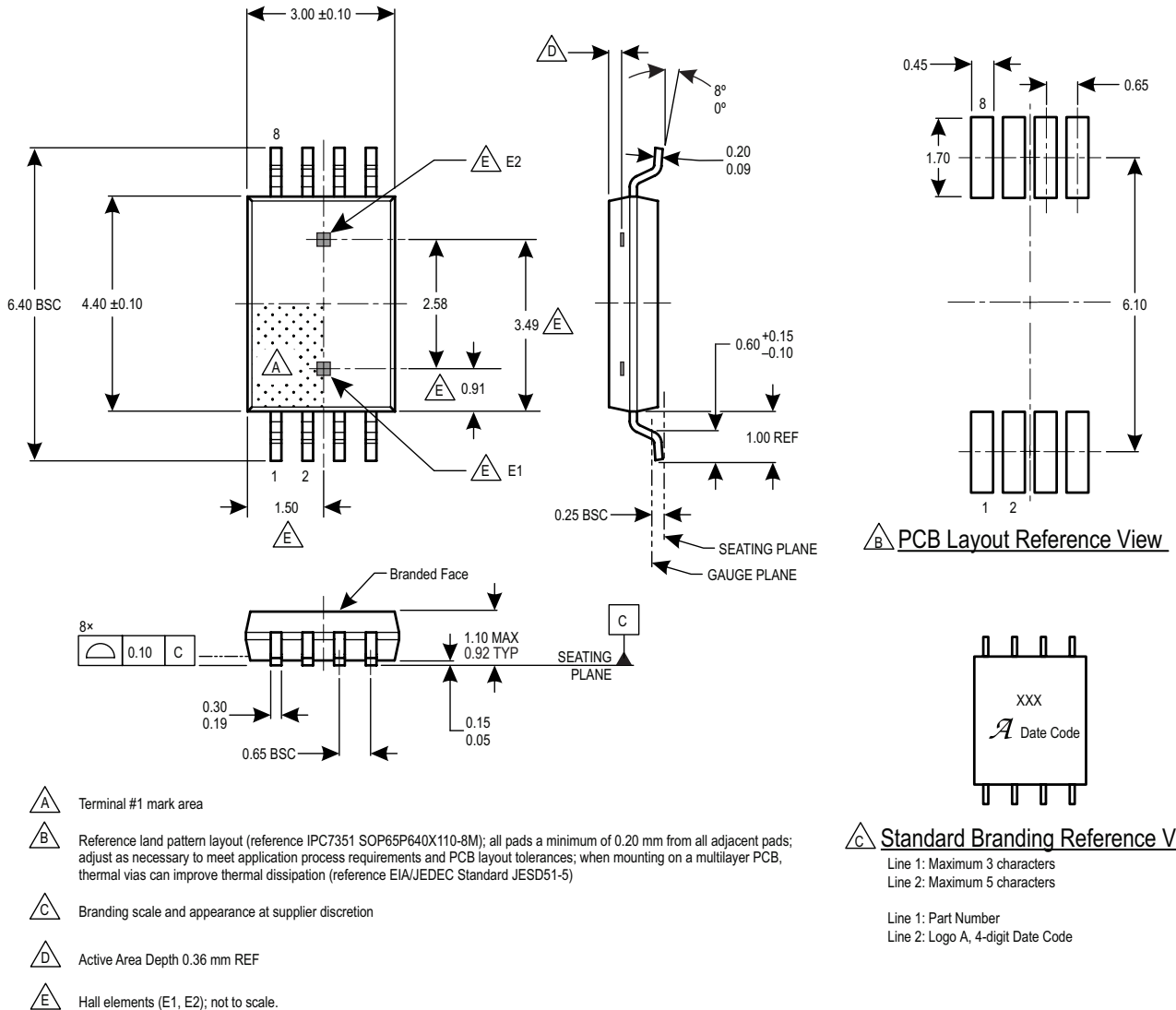


Figure 53: Package LU, 8-Pin TSSOP Package

Revision History

Number	Date	Description
	March 22, 2021	Advance Information
	April 14, 2022	Preliminary
	August 31, 2022	Changes to: bandwidth options and minor editorial adjustments (page 1); product selection guide (page 2); power-on reset hysteresis, internal bandwidth, and rise time characteristics (page 8); propagation delay and response time characteristics (page 9); nonlinearity performance characteristics (pages 11–15); QVO parameters (page 24); and Overcurrent Fault Qualifier table (page 28)
–	December 8, 2022	Initial release to EtQ, with the following changes: Removed preliminary/confidential markings (throughout); removed references to 300 kHz option (throughout); Updated human body model ESD rating (page 4); Updated output voltage clamp and broken wire voltage (page 9); Updated performance characteristics, including noise, sens ratiometry error, sensitivity drift over temperature, QVO ratiometry error, quiescent voltage output temperature error, QVO lifetime drift, and sens lifetime drift (pages 11 – 15); updated read acknowledge (device to controller) fields (page 20); removed sensitivity fine footnote (page 24); added guidance for best response over frequency and amended reference busbar design (page 36); Added typical height and Allegro reference number to package outline drawing (page 39)

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