A80804 and A80804-1

High-Current Four-Channel Automotive LED Controller

FEATURES AND BENEFITS

- AEC-Q100 qualified
- V_{IN} range: 5.3 to 40 V supply, operates down to 5.1 V when enabled
- Four independent MOSFET drivers
- Internal and external PWM dimming options
  - □ Internal PWM dimming set by resistor divider or analog voltage
  - □ External PWM dimming set by microcontroller
- Flexible LED analog dimming options
  - □ Two ADIM pins for LED binning, NTC feedback, or hybrid analog/PWM dimming
  - □ Adjustable integrated LED current derating for elevated V_{IN}
  - □ Integrated LED current derating for elevated IC junction temperature
- Combine A80804 devices in parallel for higher number of LED strings; PWMOUT signal available when used with internal PWM for master/slave operation
- MINOUT signal available to trim a pre-regulator to minimize power loss
- Selectable LED current slew rate limit during PWM dimming
- Extensive fault detection and protection
  - □ Drain short-to-ground detection
  - □ Drain short-to-VIN
  - □ Open LED
  - □ Thermal protection
  - □ Programmable input UVLO

DESCRIPTION

The A80804 and A80804-1 are linear, programmable current controllers capable of accurately regulating current in four LED strings using external MOSFETs. Each of the four LED drivers has an independent enable/PWM input and current-sense resistors and can be independently dimmed with an external PWM signal, or all channels can be dimmed with internal PWM dimming and automatic phase shifting. The overall LED current can be switched between low and full intensity for applications including stop/tail or DRL/position lighting. Multiple analog dimming options are available to support applications including LED binning, NTC foldback, or hybrid dimming. A selectable LED current slew-rate control is available to tune PWM edge times and improve EMI performance.

The MINOUT feature allows for trimming an external DC-DC converter to optimize the voltage across the linear current regulating MOSFETs to minimize power loss.

The A80804 offers several fault detection and protection options including MOSFET drain short-to-ground, drain short-to-VIN, open-LED fault protection, internal overtemperature protection, and undervoltage lockout. The A80804 can be configured for either one-out-all-out or one-out-continue operation.

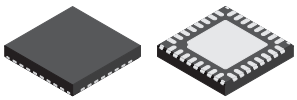
The A80804 has a 500 mV current-sense reference for improved BCI performance. The A80804-1 has a 200 mV current-sense reference for lower power dissipation in the sense resistor.

The device is packaged in a 32-pin QFN (ET) with exposed pad for enhanced thermal dissipation and wettable flank construction for solderability and visual inspection.

APPLICATIONS

- Automotive medium-power LED lighting systems
- Fog lights, backup lights, daytime running lights, position lights, sequential light

PACKAGE



32-contact QFN
5 mm × 5 mm × 0.90 mm
with exposed thermal pad
and wettable flank
(suffix ET)

Not to scale

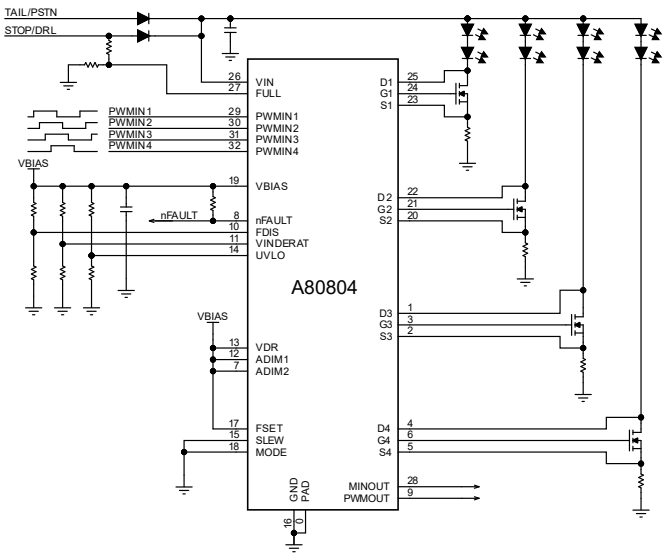


Figure 1: Typical Application Diagram with External PWM

SELECTION GUIDE

Part Number	V_{SENSE} Option (mV)	Package	Packing [1]
A80804KETASR	500	32-pin 5 mm × 5 mm QFN with exposed thermal pad and wettable flank	1500 pieces per 7-inch reel
A80804KETASR-1	200		

[1] Contact Allegro for additional packing options.

ABSOLUTE MAXIMUM RATINGS [2]

Characteristic	Symbol	Notes	Rating	Unit
VIN, FULL, nFAULT, PWMINx, Dx, Gx, and MINOUT Pins			–0.3 to 45	V
All other pins			–0.3 to 7	V
Maximum Continuous Junction Temperature	$T_{J(MAX)}$		150	°C
Transient Junction Temperature	T_J		175	°C
Storage Temperature Range	T_{stg}		–55 to 150	°C

[2] Stresses beyond those listed in this table may cause permanent damage to the device. The absolute maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions [3]	Value	Unit
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	On 4-layer PCB based on JEDEC standard	30	°C/W

[3] Additional thermal information available on the Allegro website.

Table of Contents

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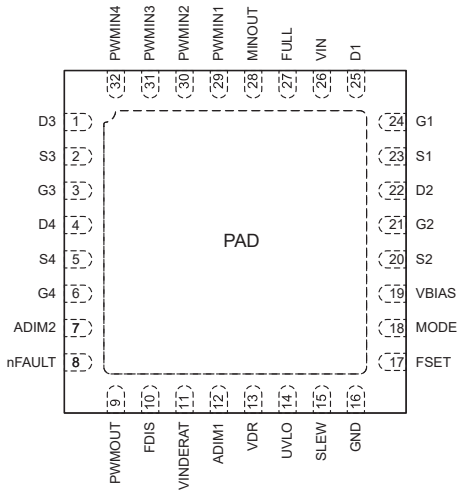
TERMINAL DIAGRAM AND TERMINAL LIST



ET-32 Package Terminals

Terminal List

Number	Name	Function
1	D3	Drain sensing for channel 3 for LED fault detection.
2	S3	Current sense for channel 3; connect sense resistor to GND to set peak current level.
3	G3	Gate driver for external N-channel MOSFET for channel 3.
4	D4	Drain sensing for channel 4 for LED fault detection.
5	S4	Current sense for channel 4; connect sense resistor to GND to set peak current level.
6	G4	Gate driver for external N-channel MOSFET for channel 4.
7	ADIM2	Voltage on this pin sets peak LED current. This pin can be used for external thermal derating using an NTC, or “hybrid” analog and PWM dimming to extend the range of PWM duty cycles.
8	nFAULT	Open-drain active low fault flag output; also used as fault input when MODE is connected to VBIAS.
9	PWMOUT	Replicated internal PWM dimming frequency and duty cycle signal for cascaded driver applications. Leave PWMOUT pin open if it is not used. PWMOUT is not driven in external PWM mode.
10	FDIS	VIN threshold for LED Open fault detection.
11	VINDERAT	Voltage at this pin sets VIN derating threshold.
12	ADIM1	Voltage on this pin sets peak LED current. This pin can be used for LED binning adjustment.
13	VDR	Voltage on this pin sets the internal PWM dimming duty cycle.
14	UVLO	Voltage at this pin sets the input voltage UVLO threshold.
15	SLEW	Controls rise and fall times of LED current. Tie to VBIAS to drive LEDs with 80 µs slew time or tie to GND to drive LEDs with 6 µs slew time. Connect a resistor to GND to adjust slew time between this range.
16	GND	Ground.
17	FSET	Sets internal PWM dimming frequency. Connect a resistor to GND to set internal PWM frequency; connect to VBIAS when using external PWM.
18	MODE	Sets the fault handling mode. Tie to VBIAS for "one-out-all-out" or the GND for "One-Out-Continue". See Table 1.
19	VBIAS	Internal bias supply; connect to GND through a 2.2 µF / 16 V ceramic capacitor. VBIAS pin can deliver up to 10 mA to an external load.
20	S2	Current sense for channel 2; connect sense resistor to GND to set peak current level.
21	G2	Gate driver for external N-channel MOSFET for channel 2.
22	D2	Drain sensing for channel 2 for LED fault detection.
23	S1	Current sense for channel 1; connect sense resistor to GND to set peak current level.
24	G1	Gate driver for external N-channel MOSFET for channel 1.
25	D1	Drain sensing for channel 1 for LED fault detection.
26	VIN	Input supply; place a 0.1 µF decoupling capacitor close to this pin.
27	FULL	Drive high to override PWM settings and force all enabled LED channels to 100% duty cycle; drive low for LEDs to operate in PWM mode. In external PWM mode, if any PWMINx pin is low at startup, the FULL pin must be low for at least 20 ms.
28	MINOUT	Provides minimum drain voltage of enabled channels during LED on-time; use for feedback to adjust the output of a pre-regulator.
29	PWMIN1	External PWM input for LED channel 1; tie this pin high for 100% duty cycle or to use internal dimming.
30	PWMIN2	External PWM input for LED channel 2; tie this pin high for 100% duty cycle or to use internal dimming.
31	PWMIN3	External PWM input for LED channel 3; tie this pin high for 100% duty cycle or to use internal dimming.
32	PWMIN4	External PWM input for LED channel 4; tie this pin high for 100% duty cycle or to use internal dimming.
–	PAD	Exposed thermal pad; connect to external ground pad for better thermal performance.

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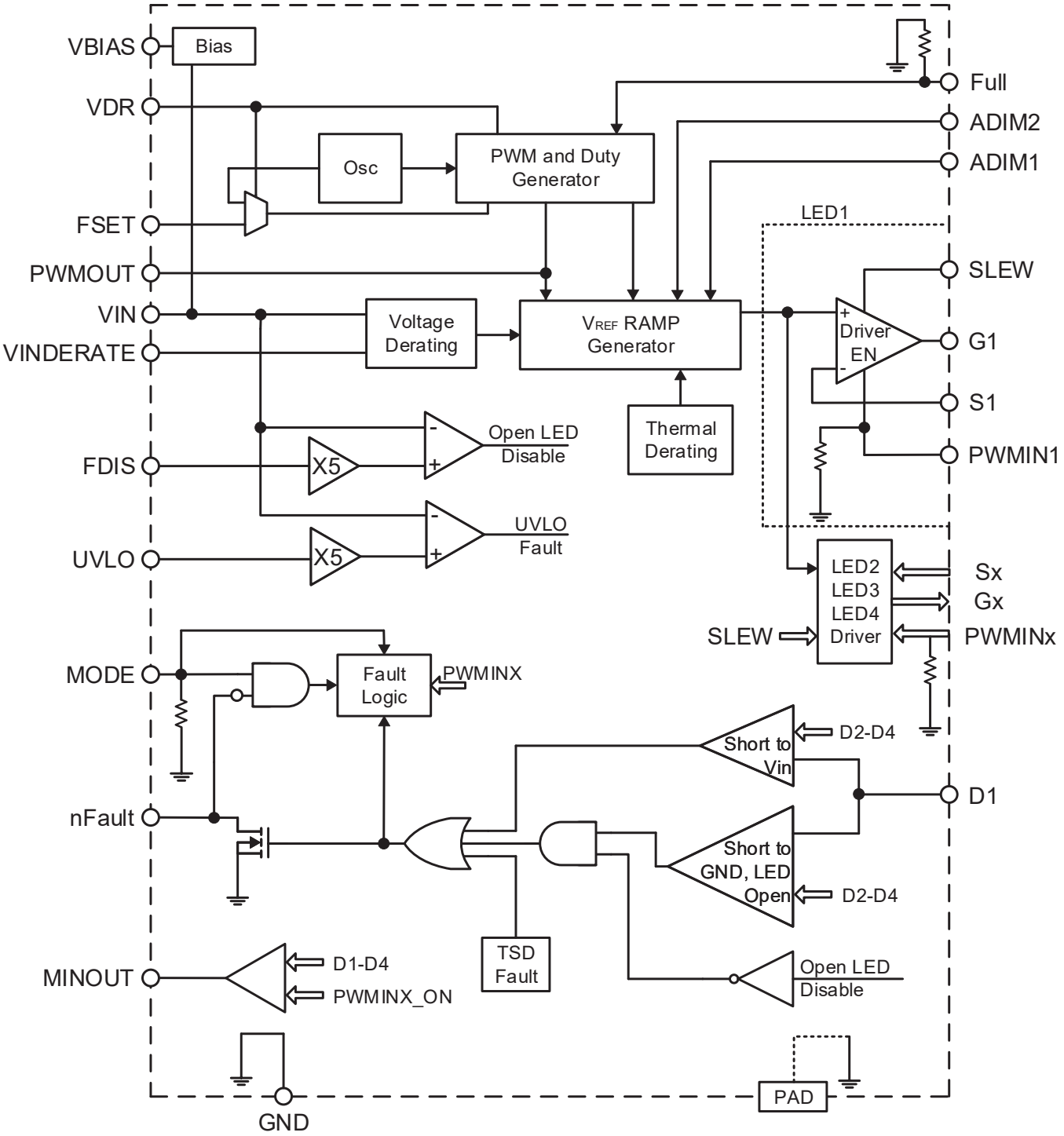
FUNCTIONAL BLOCK DIAGRAM



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ELECTRICAL CHARACTERISTICS [1]: Unless otherwise specified, V_{IN} = 12 V. "•" indicates specifications across the full operating temperature range of T_J = –40°C to 150°C; other specifications are at T_J = 25°C, unless noted otherwise. Refer to Figure 23 in application information section for typical application.

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
INPUT SUPPLY							
Operating Input Voltage Range	V_{IN}		•	5.3	–	40	V
V_{IN} Operational Current	I_{INQ}	FULL = HIGH	•	–	–	10	mA
Startup Time	t_{ON}	C_{VBIAS} = 2.2 µF, $V_{INDERAT}$ = V_{ADIMx} = V_{BIAS}, V_{SX} = 20 mV (A80804-1), V_{SX} = 50 mV (A80804), V_{IN} = 12 V, PWMINx toggled high.		–	100	–	µs
CURRENT REGULATION							
Sx Reference Voltage	V_{SENSE}	A80804-1; $V_{VINDERAT}$ = V_{ADIMx} = V_{VBIAS}	•	194	200	206	mV
		A80804-1; $V_{VINDERAT}$ = V_{ADIMx} = V_{VBIAS} (T_J = 125°C)		196	200	204	mV
		A80804; $V_{VINDERAT}$ = V_{ADIMx} = V_{VBIAS}	•	485	500	515	mV
		A80804; $V_{VINDERAT}$ = V_{ADIMx} = V_{VBIAS} (T_J = 125°C)		490	500	510	mV
Sx Reference Matching [1]	Err_{VSENSE}	No derating		–	–	2	%
Analog Dimming ADIM1 / VBIAS Ratio	ADIM1R	V_{ADIM2} = V_{VBIAS}, no derating, V_{SX} = 180 mV (A80804-1), V_{SX} = 450 mV (A80804)		–	0.72	–	–
Analog Dimming ADIM2 / VBIAS Ratio	ADIM2R	V_{ADIM1} = V_{VBIAS}, no derating, V_{SX} = 180 mV (A80804-1), V_{SX} = 450 mV (A80804)		–	0.45	–	–
VBIAS							
VBIAS Pin Voltage	V_{VBIAS}	I_{VBIAS} = 0 to 10 mA	•	4.85	5.0	5.15	V
VBIAS Undervoltage Release	$V_{VBIASUV}$	V_{IN} rising		–	4.5	–	V
VBIAS Undervoltage Lockout Hysteresis	$V_{VBIASHYS}$	IC disabled		–	0.2	–	V
GATE DRIVER							
Gx High-Level Output	V_{GATEH}	V_{IN} = 12 V, Gx High, V_{SX} = 180 mV (A80804-1) and V_{SX} = 450 mV (A80804)		6	–	9	V
Gx Low-Level Output	V_{GATEL}	FSET = VBIAS, PWMIN = LOW		–	–	0.7	V
GATE Driver Dropout	V_{GATE_drop}	V_{IN} = 5.3 V, V_{SX} = 180 mV (A80804-1) and V_{SX} = 450 mV (A80804), measured as (V_{IN} – V_{GX})		–	–	1	V
Gate Pull-Up Current	I_{GPU}	V_{SX} = 180 mV (A80804-1) and V_{SX} = 450 mV (A80804), V_{GX} = 0 V, V_{IN} = 7 V		–	–360	–	µA
Gate Pull-Down Current	IGPD	V_{SX} = 220 mV (A80804-1) and V_{SX} = 550 mV (A80804), V_{GX} = 7 V, V_{IN} = 7 V		–	360	–	µA
External FET Gate Capacitance Range [4]	C_{GISS}	For stable operation		250	–	2000	pF
Propagation Delay	t_{pdi}	Delay from Internal PWM and PWMOUT pin during internal PWM mode.		–	2	–	µs
Propagation Delay, External PWM Mode	t_{pde}	Delay from PWMINx pin rising or falling level to Gx rising 3 V; C_{gate} = 1 nF		–	2	–	µs
PWM Matching During External PWM		Duty cycle mismatch at 5%, 200 Hz PWM signal applied on PWMINx pins		–	–	6	%
PWM Dimming Frequency	f_{PWM}	R_{FPWM} = 30.9 kΩ, across FSET to GND	•	180	200	220	Hz

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ELECTRICAL CHARACTERISTICS [1] **(continued):** **Unless otherwise specified, V_{IN} = 12 V. "•" indicates specifications across the full operating temperature range of T_J = –40°C to 150°C; other specifications are at T_J = 25°C, unless noted otherwise. Refer to Figure 23 in application information section for typical application.**

Characteristics	Symbol	Test Conditions			Min.	Typ.	Max.	Unit
GATE DRIVER (continued)								
Internal PWM Duty Cycle	D_{PWML}	V_{DR} driven by resistor divider from VBIAS, f_{PWM} = 200 Hz,	V_{VBIAS} / V_{DR} = 73 V, SLEW = Low		1	2	3	%
			V_{VBIAS} / V_{DR} = 29.2 V, SLEW = Low		4.25	5	5.8	%
	D_{PWMH}	V_{DR} driven by resistor divider from VBIAS, V_{VBIAS} / V_{DR} = 1.62 V, f_{PWM} = 200 Hz	SLEW = Low		88	90	92	%
			SLEW = High		88	90	92	%
Current Slew Time	t_{SLEW}	Rising or falling between 10% and 90% levels, for internal reference ramp	SLEW = High		49	80	111	µs
			SLEW = Low		4	8	12	µs
			R_{SLEW} = 100 kΩ		14	25	36	µs
Rise Time to Fall Time Matching [2]	t_{SM}	Rising or falling between 10% and 90% levels, for internal PWM; SLEW = High			–	20	–	µs
		Rising or falling between 10% and 90% levels, for external PWM; SLEW = High			–	20	–	µs
Rise Time and Fall Time Mismatch Between Four Strings [3][4]	t_{SMS}	Rise and fall time mismatch between 10% and 90% levels in four strings; SLEW = High			–	3	–	%
INTERNAL PWM POLYPHASE DELAY								
Poly-Phase Delay	t_{dpp}	Internal PWM, delay between rise and fall times of successive outputs; measured at 50% V_{SENSE} levels			–	100	–	µs
LOGIC PINS								
MODE, SLEW, FSET, PWMINX, nFAULT, FULL Pins, Input Low Voltage	V_{IL}	Below V_{IL} level, input voltage considered as logic low		•	0.8	–	1.1	V
MODE, SLEW, FSET, PWMINX, nFAULT, FULL Pins, Input High Voltage	V_{IH}	Above V_{IH} level, input voltage considered as logic high		•	1.5	–	2	V
nFAULT, PWMOUT Pins, Output Low Voltage	V_{OL}	I_{OL} = 1 mA		•	–	–	0.4	V
PWMOUT Pin, Output High Voltage	V_{OH}	I_{OH} = –1 mA		•	4	–	–	V
MODE, PWMINx, FULL, Pin Pull-Down Resistor	R_{in}				–	100	–	kΩ
PROTECTION								
Input Voltage Required to Derate VSENSE by 10%	$V_{INth(L)}$	$V_{INDERAT}$ = 2 V			19.7	20.7	21.7	V
V_{IN} Derating Range ($V_{INth(H)}$ to $V_{INth(L)}$)	V_{INthd}	V_{SENSE} drops from 90% to 60% level			–	2.16	–	V
Maximum V_{IN} Derating for SENSE Voltage	V_{REF1}	$V_{INDERAT}$ = 2 V, V_{IN} ≥ 26 V			–	50	–	%
VIN-to-Drain Short Detect Voltage	V_{SCV}	Measured as V_{IN} – V_{Dx}, Gx = PWMINx = high		•	0.5	0.8	1.1	V
Open LED Fault Detect Voltage	V_{OLED}	Measured at Dx, V_{IN} > 5 × V_{FDSET}		•	0.19	0.24	0.29	V
Open LED Disable Input Voltage	V_{FDIS_VIN}	V_{FDIS} = 2 V			–	10	–	V

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Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
PROTECTION (continued)							
PWM Frequency In Case Of Fault On Faulty Channel (FULL and External PWM Mode)	–	Open LED or Short to Drain fault		–	500	–	Hz
PWM Duty Cycle In Case Of Fault On Faulty Channel	–			–	5	–	%
Fault Detection Time (FULL Mode)	–	Open LED or Short to Drain fault		–	6	–	ms
Fault Detection Cycles (PWM Mode)	–			–	3	–	cycles
Fault reset time (FULL or External PWM)	–			–	20	–	ms
Input Under Voltage Detect Voltage	V_{UVLO}	V_{UVLO} = 2 V, V_{IN} Falling (5×)		–	10	–	V
Input Under Voltage Detect Voltage Hysteresis	$V_{UVLOhys}$	V_{IN} rising (fixed)		–	0.8	–	V
Thermal Monitor Activation Temperature [4]	T_{JM}	T_J at V_{SENSE} = 180 mV (A80804-1) and V_{SENSE} = 450 mV (A80804)		–	T_{JF} – 21	–	°C
Thermal Monitor Low Current Temperature [4]	T_{JL}	T_J at V_{SENSE} = 70 mV (A80804-1) and V_{SENSE} = 175 mV (for A80804)		–	T_{JF} – 7	–	°C
Overtemperature Shutdown [4]	T_{JF}	Temperature increasing		–	170	–	°C
Overtemperature Hysteresis [4]	T_{Jhys}	Recovery = T_{JF} – T_{Jhys}		–	30	–	°C
MINOUT							
MINOUT Internal Reference Voltage	V_{MINOUT}			–	0.8	–	V
MINOUT Drive Capability	I_{MINOUT}			–	±100	–	µA
MINOUT Gain	A_{MINOUT}			–	10	–	–
MIONOUT Offset	V_{NIMOUT_off}			–	0.5	–	V

[1] Reference matching is defined as: ($V_{SENSEmax}$ – $V_{SENSEmin}$) / $V_{SENSE(AVG)}$, where $V_{SENSE(AVG)}$ is the average of all enabled V_{SENSEx}.
[2] Rise Time to Fall Time Matching is defined as the maximum difference between the rise time and the fall time of the same string.
[3] Rise Time to Fall Time Mismatch Between Four Strings is defined as the maximum ratio of the difference between either the rise time or the fall time to the average of the rise time or fall times between four strings.
[4] Ensured by design and characterization.

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FUNCTIONAL DESCRIPTION

The A80804 is a four-channel linear current regulator for LED driver applications using external N-channel MOSFETs to handle power dissipation in linear mode. The LED current in each channel can be programmed separately by selecting each current-sense resistor. Each channel also has a separate PWMINx pin to control external PWM dimming or act as an enable pin. The peak LED current can be further controlled by analog dimming using ADIM1 and ADIM2.

Internal PWM generation uses a resistor to ground on FSET to set the PWM frequency and a voltage on VDR to set the duty cycle, typically a resistor divider from VBIAS to ground. When using internal PWM, the PWM signal is replicated on the PWMOUT pin for cascading multiple A80804s together.

For external PWM mode, connect FSET to VBIAS and apply a PWM signal to each PWMINx pin. The PWMOUT pin stays low while using external PWM.

Extensive protections such as input undervoltage, MOSFET drain short-to-GND, drain short-to-VIN, LED open, and thermal shutdown are incorporated to protect the device and the LEDs. The A80804 also includes LED current derating for high input voltages, based on a programmable threshold, and high internal device temperature.

LED Current Sense Resistor

LED peak current (100%) level can be set independently for each channel by selecting a proper resistor value from each Sx pin to GND as shown in Equation 1:

Equation 1:

$$I_{LEDpeak} = V_{SENSE} / R_{SENSE}$$

where V_{SENSE} is 500 mV for A80804 devices and 200 mV for A80804-1 devices, $I_{LEDpeak}$ is in amps (A), and R_{SENSE} is in Ω.

LED PWM Dimming

A80804 can operate in external PWM mode where each channel can be individually controlled or in internal PWM dimming mode with automatic phase shifting. Tie the FSET pin to VBIAS to use external PWM mode or tie to GND through a resistor for internal PWM mode.

External PWM Dimming

When FSET is tied to VBIAS, the A80804 operates in external PWM mode. A logic-level input signal can be used to control each PWMINx pin to set each respective channel's PWM frequency and duty cycle, allowing each channel to be dimmed independently.

The external PWM frequency should be between 200 Hz and 1000 Hz with a duty cycle between 5% and 100%. While in external PWM mode, the PWMOUT pin will stay low.

The LEDs turn on when each respective PWMINx signal is high. The LED current slew rate is controlled through the SLEW pin and the same slew control is applied to all channels.

For wider dimming ratios, external PWM dimming can be combined with analog dimming.

Internal PWM Dimming

To use the A80804 with internal PWM dimming and automatic phase shifting between each channel, tie the FSET pin to GND through a resistor to set the PWM frequency. The internal PWM frequency range is 100 to 1000 Hz. Use Equation 2 to calculate the resistor value for a PWM frequency.

Equation 2:

$$R_{FPWM} = 5400 / (f_{PWM} - 25)$$

where f_{PWM} is in Hz and R_{FPWM} is in kΩ.

For example, for f_{PWM} = 200 Hz, use a 30.9 kΩ resistor.

The internal PWM dimming duty cycle is set with a voltage on the VDR pin. The PWM duty cycle depends on the ratio of the voltage at the VDR and VBIAS pins. For better accuracy, use a voltage divider from VBIAS to VDR. The internal duty cycle range is 2% to 90%. See Equation 3 and Figure 2.

Equation 3:

$$DUTY = 146 \times V_{DR} / V_{BIAS}$$

where V_{DR} and V_{BIAS} are in volts and DUTY is the duty cycle in percent.

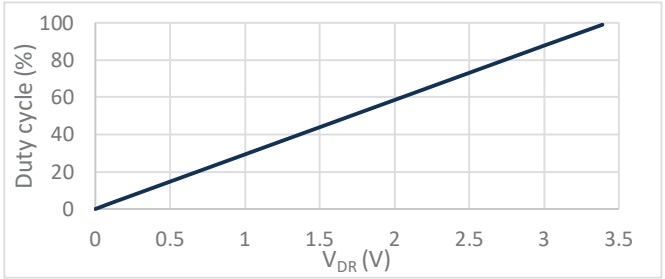

Figure 2: Relationship of External Voltage Input on VDR Pin and Dimming Duty Cycle. V_{DR} can be varied from 0 to 3.6 V.

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Internal PWM Phase Shift

While operating in internal PWM mode, the signal sent to the first channel is delayed 100 µs (typical) from the internal reference PWM signal, and each subsequent channel is delayed another 100 µs (typical) from the previous channel to minimize di/dt and improve EMI. If any channel is not used, the delay for the remaining channels will remain the same. For example, if channel 1 and 2 are not used, channel 3 and 4 will still be delayed by 300 µs and 400 µs with respect to the internal PWM signal.

Equation 4:

$$t_{CHDELAY} = 100\ \mu s \times N$$

where N is the channel number.

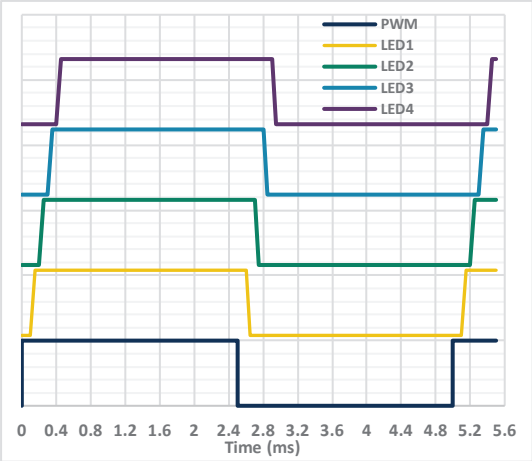

Figure 3: Polyphase Operation with Internal PWM

The polyphase behavior is disabled in external PWM mode since each channel can be independently controlled, and each channel's PWMINx signal can be time-shifted to achieve polyphase operation.

Full Mode

When the FULL pin is pulled high, the A80804 ignores the PWM configuration and operates at 100% duty cycle. The FULL pin does not affect the analog dimming level.

Analog Dimming

Analog dimming is available through ADIM1 and ADIM2. Each ADIMx pin can be tied to VBIAS to disable the dimming for that ADIM pin. When not tied to VBIAS, the voltage on ADIMx scales V_{SENSE}, the internal reference voltage that is maintained across R_{SENSE}. The lower of the two ADIMx options will determine the dimming level. Analog dimming is ratiometric to V_{BIAS}. V_{ADIM1} is the voltage at ADIM1, and V_{ADIM2} is the voltage at ADIM2. The V_{SENSE} reference voltage is also affected by Input Overvoltage Derating and Thermal Derating and Protection Shutdown, and the V_{SENSE} level for regulation is the minimum of all of these circuits.

Analog Dimming with ADIM1

An analog voltage on ADIM1 can be used to derate the peak LED current for binning or other application requirements. While ADIM2 is at V_{BIAS}, to disable dimming on ADIM2, the reference voltage V_{SENSE} scales with ADIM1 based on Equation 5. Use Equation 6 to find the voltage at ADIM1 for a targeted dimming level.

Equation 5:

$$V_{SENSE} = 0.6371 \times (V_{ADIM1}/V_{BIAS}) - 0.0097 \text{ (A80804)}$$

$$V_{SENSE} = 0.2571 \times (V_{ADIM1}/V_{BIAS}) - 0.0057 \text{ (A80804-1)}$$

where $V_{ADIM2} = V_{BIAS}$.

Equation 6:

$$V_{ADIM1} = (V_{BIAS} \times (500\ mV \times DimPct + 0.0097)) / 0.637 \text{ (A80804)}$$

$$V_{ADIM1} = (V_{BIAS} \times (200\ mV \times DimPct + 0.0057)) / 0.2571 \text{ (A80804-1)}$$

where $V_{ADIM2} = V_{BIAS}$ and DimPct is the dimming percentage target, scaled from 0 to 1.

To use analog dimming with ADIM1, set V_{ADIM1} between 10% and 80% of V_{BIAS}; see Figure 4.

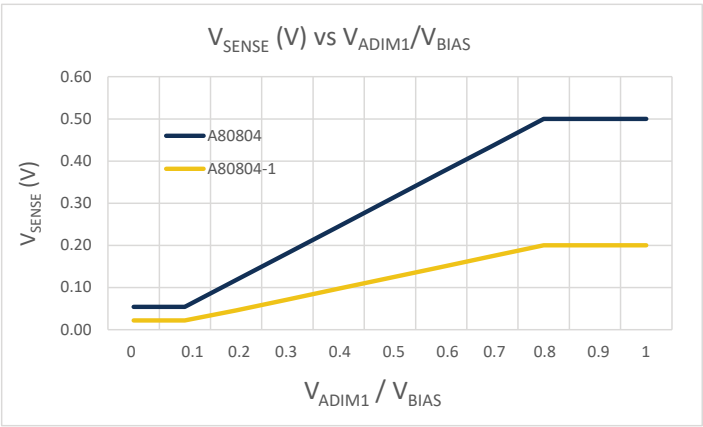

Figure 4: Effect of ADIM1 on V_{SENSE}

Analog Dimming with ADIM2

An analog voltage on ADIM2 can be used to derate the peak LED current, for example with an NTC thermistor to derate the current at high LED temperatures. To use analog dimming with ADIM2,

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set V_{ADIM2} between 10% to 50% of V_{BIAS}; there is no derating when V_{ADIM2} is higher than V_{BIAS} / 2. See Equation 7 to calculate V_{SENSE} and Equation 8 to calculate the ADIM2 pin voltage for a targeted dimming ratio.

Equation 7:

$$V_{SENSE} = 1.125 \times (V_{ADIM2}/V_{BIAS}) - 0.0625 \text{ (A80804)}$$

$$V_{SENSE} = 0.450 \times (V_{ADIM2}/V_{BIAS}) - 0.025 \text{ (A80804-1)}$$

where $V_{ADIM1} = V_{BIAS}$, and $V_{ADIM2} / V_{BIAS} < 0.5$.

Equation 8:

$$V_{ADIM2} = (V_{BIAS} \times (500\ mV \times DimPct + 0.0625)) / 1.125 \text{ (A80804)}$$

$$V_{ADIM2} = (V_{BIAS} \times (200\ mV \times DimPct + 0.025)) / 0.450 \text{ (A80804-1)}$$

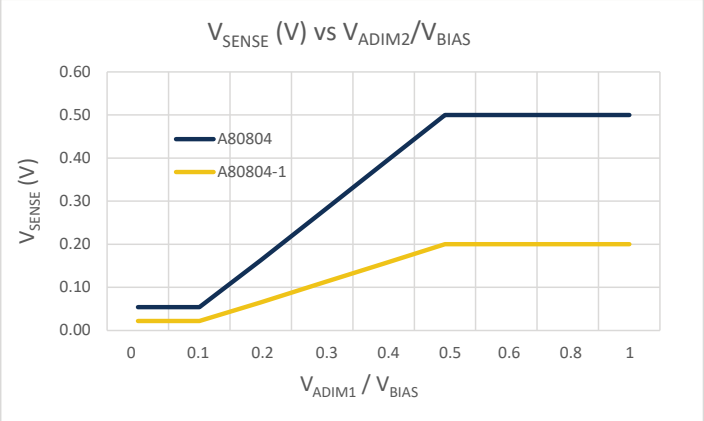

Figure 5: Effect of ADIM2 on V_{SENSE}

When both ADIM1 and ADIM2 are used, V_{SENSE} is the minimum of ADIM1 and ADIM2.

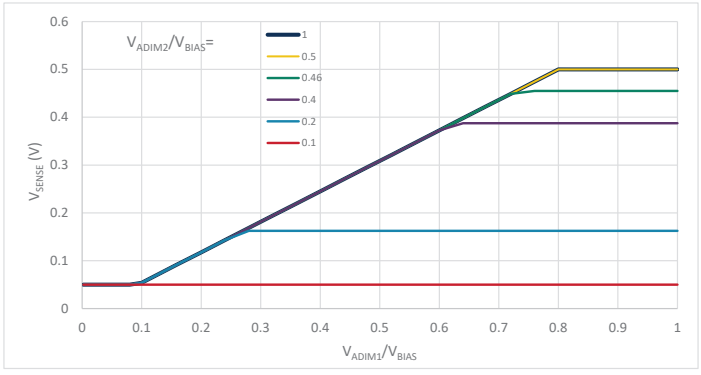

Figure 6: Combined Effect of ADIM1 and ADIM2 pin voltages on V_{SENSE} for A80804

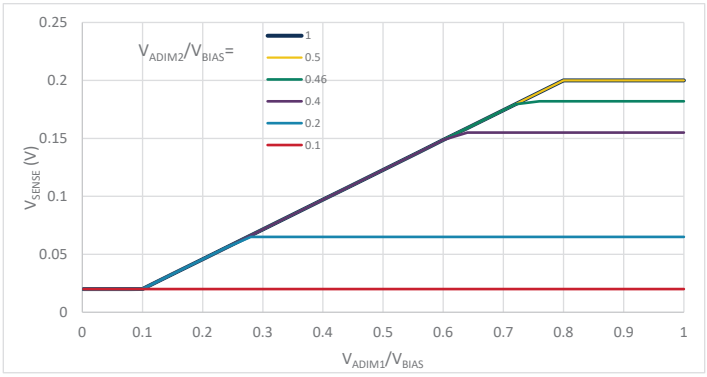

Figure 7: Combined Effect of ADIM1 and ADIM2 pin voltages on V_{SENSE} for A80804-1

LED Current Slew Control

The LED current rise and fall times can be controlled with the SLEW pin. This allows the system designer to optimize for PWM duty cycle accuracy or EMI performance. When SLEW is tied to logic high, the 10% to 90% slew time is 80 µs, the slowest slew rate option. When SLEW is connected to logic low, the slew time is 6 µs, the fastest slew rate option. For a slew rate between the low and high levels, connect SLEW to GND through a resistor using Equation 9.

Equation 9:

$$t_{SLEW} = R_{SLEW} / 4$$

where t_{SLEW} is in µs and R_{SLEW} is in kΩ. Use a value of R_{SLEW} between 324 kΩ (80 µs) and 24.3 kΩ (6 µs).

PWMOUT

The A80804 has a PWMOUT pin that replicates the reference PWM signal used while in internal PWM mode. This signal can be used as the PWMINx signal for slave devices to synchronize the slave device with the master device. Since the PWMINx pins are driven from PWMOUT, the slave device must operate in external PWM mode. Therefore, the slave device will not have the PWM channel phase shifting but uses the master's internal PWM reference which is 100 µs ahead of the channel 1 on the master; see the Multiple A80804 Master-Slave Arrangement application.

PWMOUT is low while in external PWM mode.

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MINOUT

The MINOUT pin provides an output voltage proportional to the minimum voltage of the Dx pins for all active channels. The voltage from MINOUT can be fed to a voltage regulator's feedback pin to complete a closed-loop system and trim the regulated output leading to the LEDs. The voltage on MINOUT is given by Equation 10 with minimum of 0.3 V (typical) and maximum of 3.5 V (typical).

Equation 10:

$$V_{MINOUT} = 10 \times (V_{Dx\_MIN} - 0.8) + 0.3$$

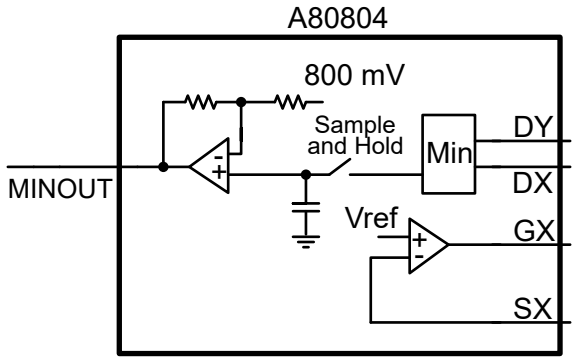

Figure 8: Block Diagram of MINOUT Block

An example of a pre-regulator powering the LED strings is shown in Figure 9. The MINOUT signal feeds into the regulator control loop through an external resistor, RFB3.

Equation 11 can be used to calculate the resistor values.

Equation 11:

$$R_{FB3} = \left[\frac{V_{MINOUT(\max)} \times (V_{OUT(max)} - V_{FB})}{V_{FB} \times (V_{OUT(max)} - V_{OUT(min)})} - 1\right] \times R_{FB2}$$

$$R_{FB1} = \left[\frac{V_{OUT(max)} - V_{FB})}{V_{FB}}\right] \times \left[\frac{R_{FB2} \times R_{FB3}}{R_{FB2} + R_{FB3}}\right]$$

$V_{OUT(min)}$ and $V_{OUT(max)}$ are the worst-case required voltages for the LEDs to operate, and V_{FB} is the feedback voltage of the pre-regulator.

Protection Functions

The A80804 asserts a fault by pulling the nFAULT pin low when a fault is detected for three consecutive PWM cycles. The 3-cycle count prevents fault assertion on a spurious transient. The device returns to normal operation immediately after the fault is removed. Any faulted LED string operates at 5% duty cycle during the PWM on-time to minimize power dissipation in the MOSFETs and detect fault recovery. While in FULL mode, the device waits 6 ms to assert the nFAULT pin low. While in external PWM mode or FULL mode, the faulted LED string is driven with a 500 Hz, 5% duty cycle PWM signal to detect fault recovery.

MODE Pin Behavior

When a fault occurs on one LED string, the behavior of other strings is determined by the state of the MODE pin. Other strings

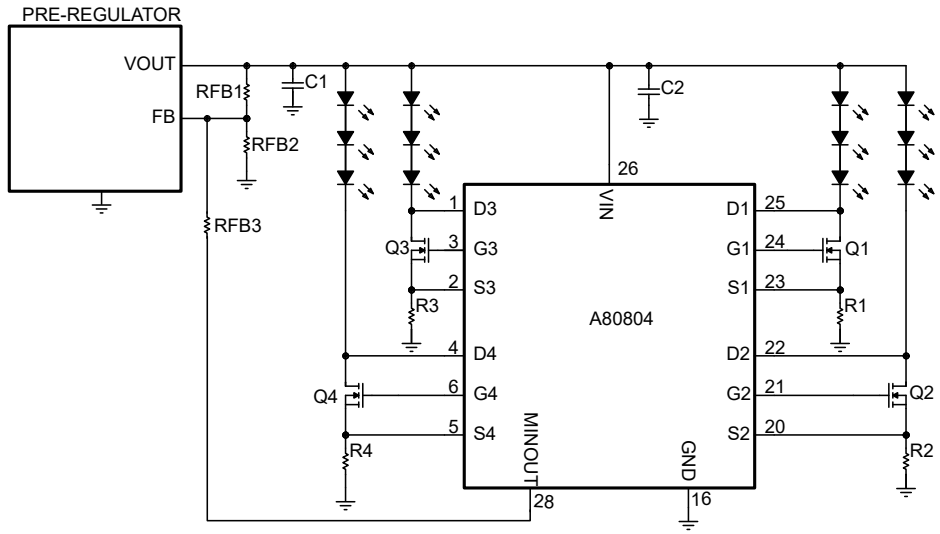

Figure 9: Example of Using MINOUT with Pre-regulator

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continue to operate normally when MODE is low ("one-out-continue" or "N-1" mode) and shutdown when MODE is high ("one-out-all-out" mode). The nFAULT pin becomes bidirectional and acts as both a fault input and output when MODE is high, which can be used to pass the fault state to slave or paralleled devices.

FDIS Pin for Fault Disable

Open LED and MOSFET drain short-to-GND faults are disabled when the input voltage is less than five times the voltage at the FDIS pin, $V_{IN} < 5 \times V_{FDIS}$. Select a V_{FDIS} level higher than the LED string's forward voltage to prevent faults during startup or V_{IN} transients.

OPEN LED

An open LED fault is detected when $V_{IN} > 5 \times V_{FDIS}$ and $V_{Dx} < 0.24$ V.

Once the fault is detected, nFAULT is asserted low and that LED channel operates with 5% duty cycle even if FULL is high, keeping the MOSFET on with a low duty cycle to detect removal of the fault for auto-recovery. The LED current in the faulted string is zero since the LED current path is open. When the fault is removed, $V_{Dx} > 0.24$ V, the device returns to normal operation.

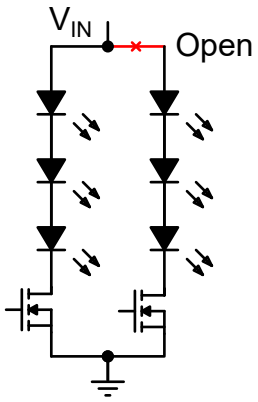

Figure 10: LED Open Protection

If MODE is high, all other gates, Gx, and PWMOUT are pulled low once the fault is detected; parallel or slave devices will also turn off when nFAULT goes low if MODE is high, or when PWMOUT is pulled low if cascading PWMOUT to PWMINx of another device. If MODE is low all other gates, Gx, and PWMOUT are unaffected and continue to operate normally.

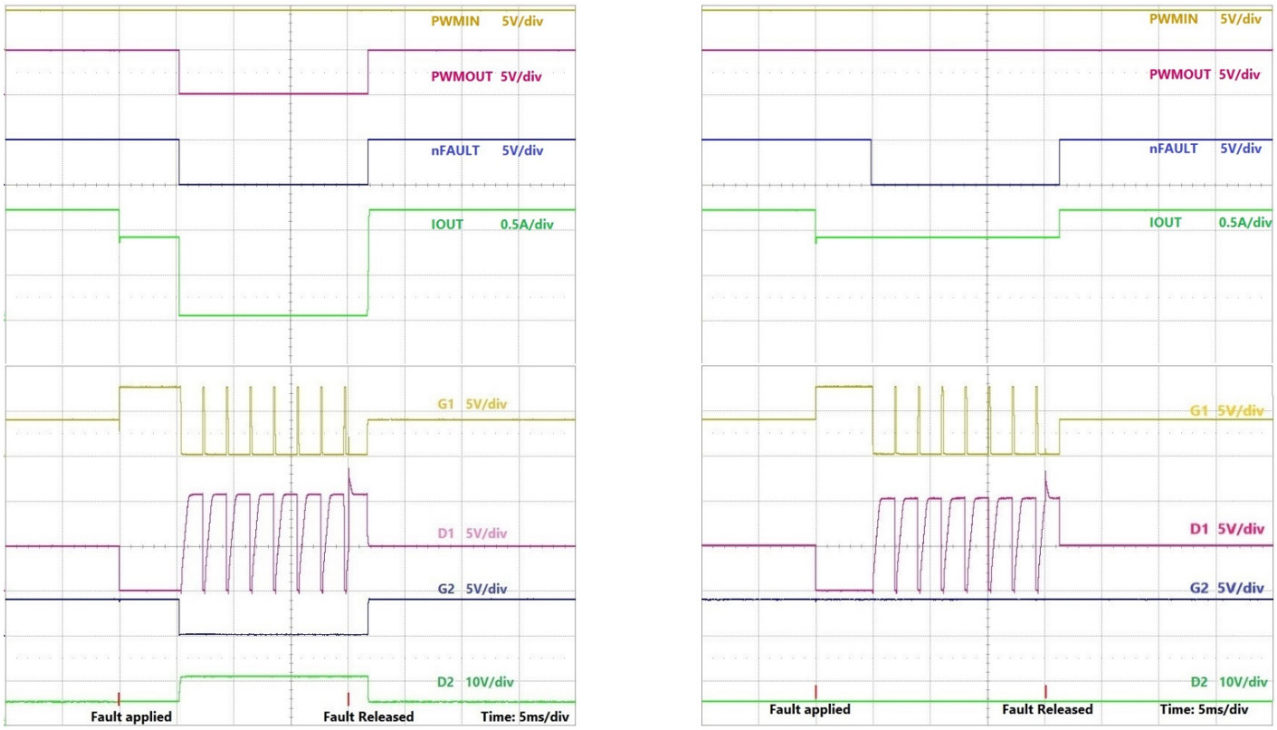

Figure 11: Open LED Fault on D1 in FULL mode. MODE = High (left), MODE = Low (right). Fault on channel 1.

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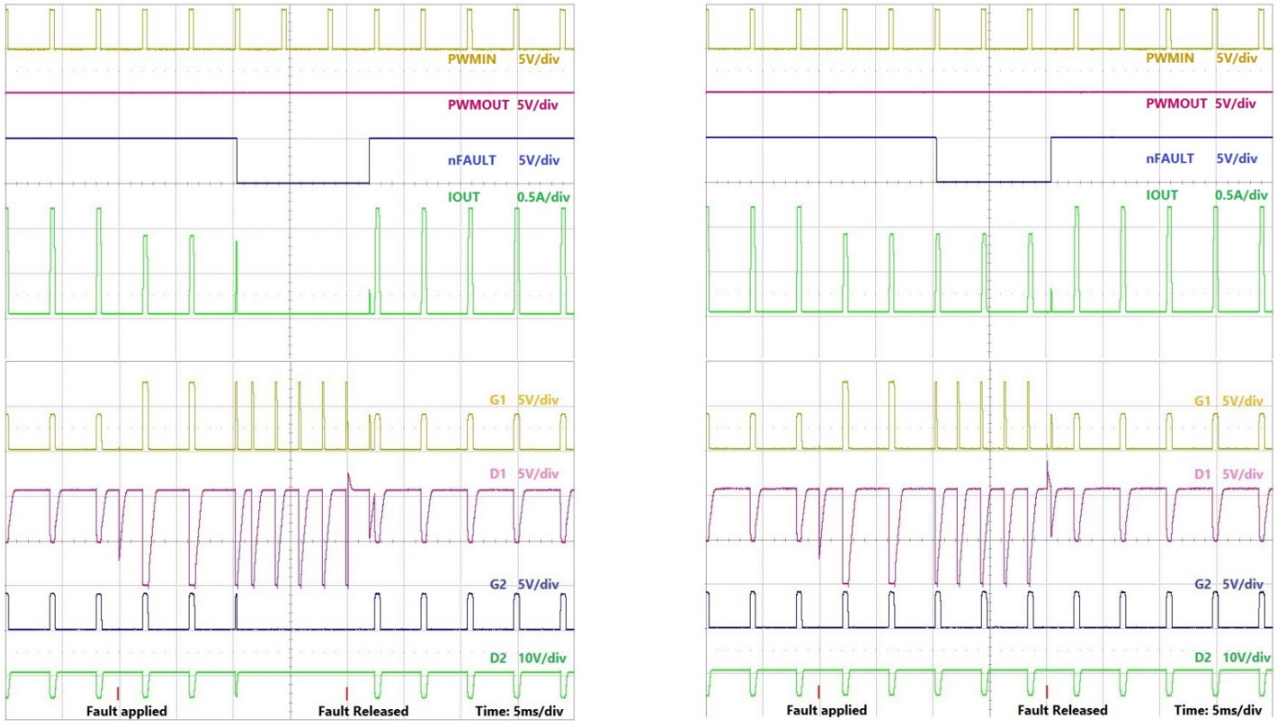

Figure 12: Open LED Fault on D1 with External PWM. Fault on channel 1. MODE = High (left), MODE = Low (right).

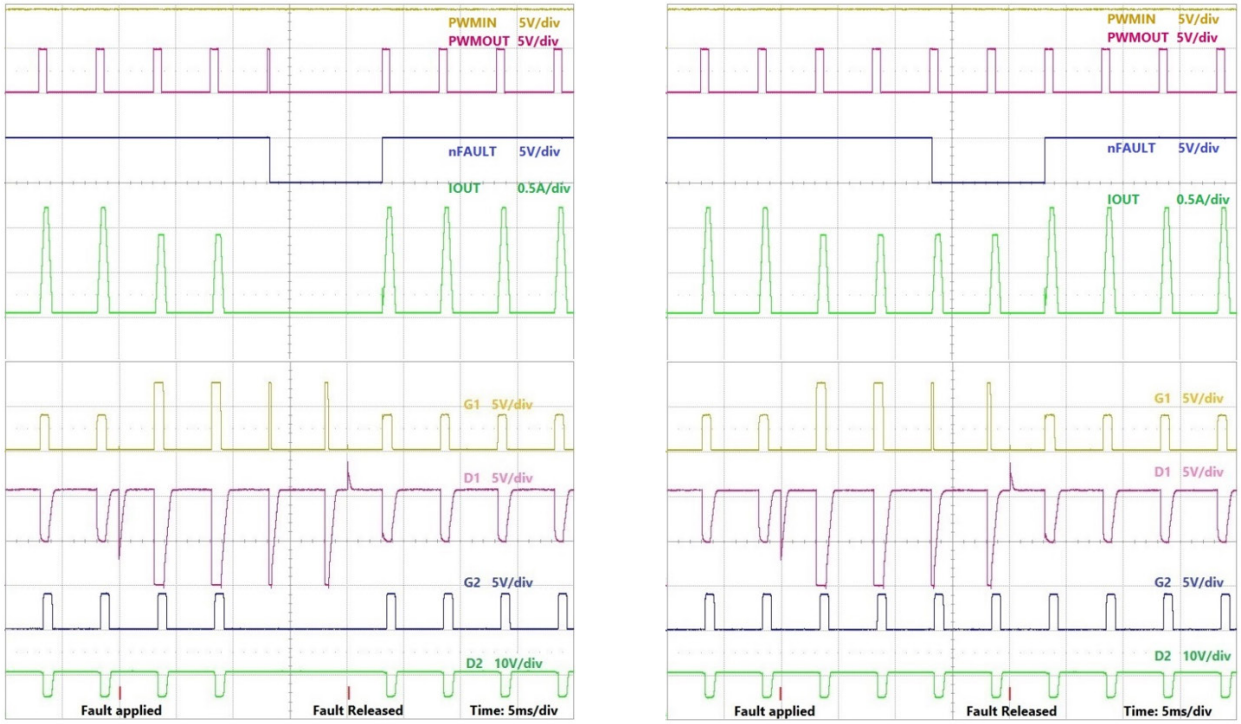

Figure 13: Open LED Fault on D1 with Internal PWM. Fault on channel 1. MODE = High (left), MODE = Low (right).

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Short Circuit Protection

The A80804 can protect against multiple short-circuit faults scenarios, as shown in Figure 14.

Drain Short To GND

A MOSFET drain short-to-ground fault is detected when $V_{IN} > 5 \times V_{FDIS}$ and $V_{Dx} < 0.24$ V. Once the fault is detected, nFAULT is asserted low and that LED channel operates with 5% duty cycle, even if FULL is high, to detect fault removal for auto-recovery. The drain short-to-ground fault is not a latched fault. When the fault is removed, $V_{Dx} > 0.24$ V, the device returns to normal operation. If MODE is high, all other gates, Gx, and PWMOUT are pulled low when the fault is detected; parallel or slave devices will also turn off when nFAULT goes low if the nFAULT pins are tied together and MODE is high. If MODE is low, the other gates and PWMOUT are unaffected and continue to operate normally. During a drain short-to-ground fault, the LED string may see a large current as the LED string is shorted to ground.

The operating waveforms Gx, Dx, PWMOUT, and nFAULT, are the same for drain short-to-GND fault and open LED fault except the faulty LED string will see large current when the drain is shorted to ground.

Drain Short To VIN

A MOSFET drain short-to-VIN, a full LED string short, is detected when $(V_{IN} - V_{Dx}) < 0.8$ V and the configured LED current slew time has elapsed while PWMINx is high. Once the fault is detected, nFAULT is asserted low and that LED channel operates with 5% duty cycle even if FULL is high, keeping the MOSFET on with a low duty cycle to detect removal of the fault for auto-recovery and minimize power dissipation in the faulty LED string. The drain short-to-VIN fault is not a latched fault. When the fault is removed, $(V_{IN} - V_{Dx}) > 0.8$ V, the device returns to normal operation. The current in the faulted LED string during the fault will be zero since the LED string is shorted out when the MOSFET drain is shorted to VIN.

If MODE is high, all other gates, Gx, and PWMOUT are pulled low once the fault is detected; parallel or slave devices will also turn off when nFAULT goes low if the nFAULT pins are tied together and MODE is high. If MODE is low, all other gates, Gx, and PWMOUT are unaffected and continue to operate normally.

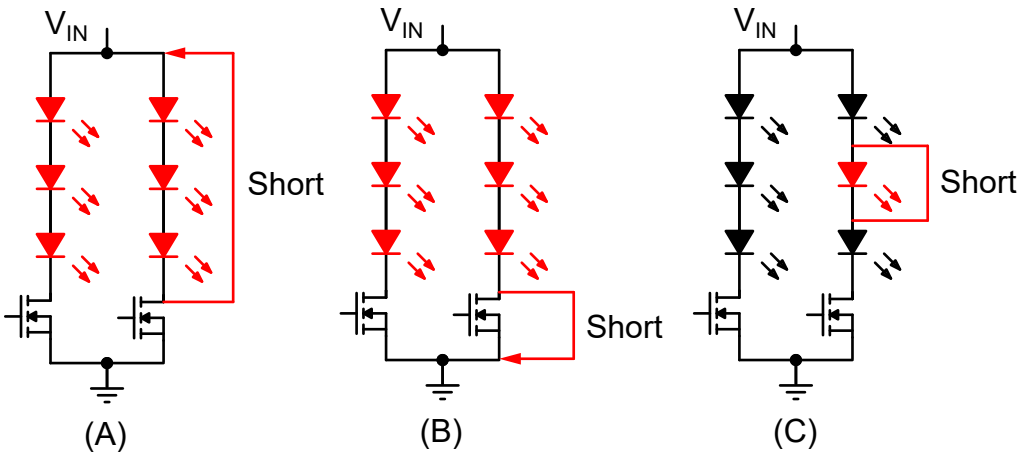

Figure 14: Short-Circuit Protection

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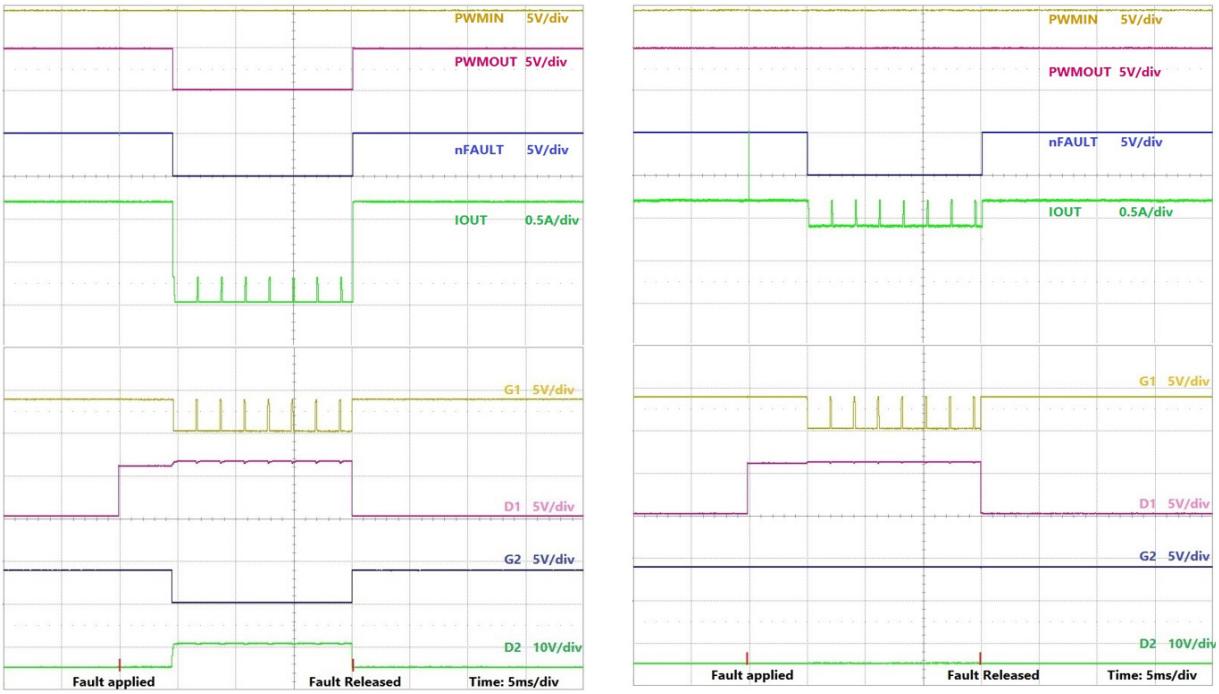

Figure 15: Drain Short to VIN Fault on D1 in FULL mode. MODE = High (left), MODE = Low (right).

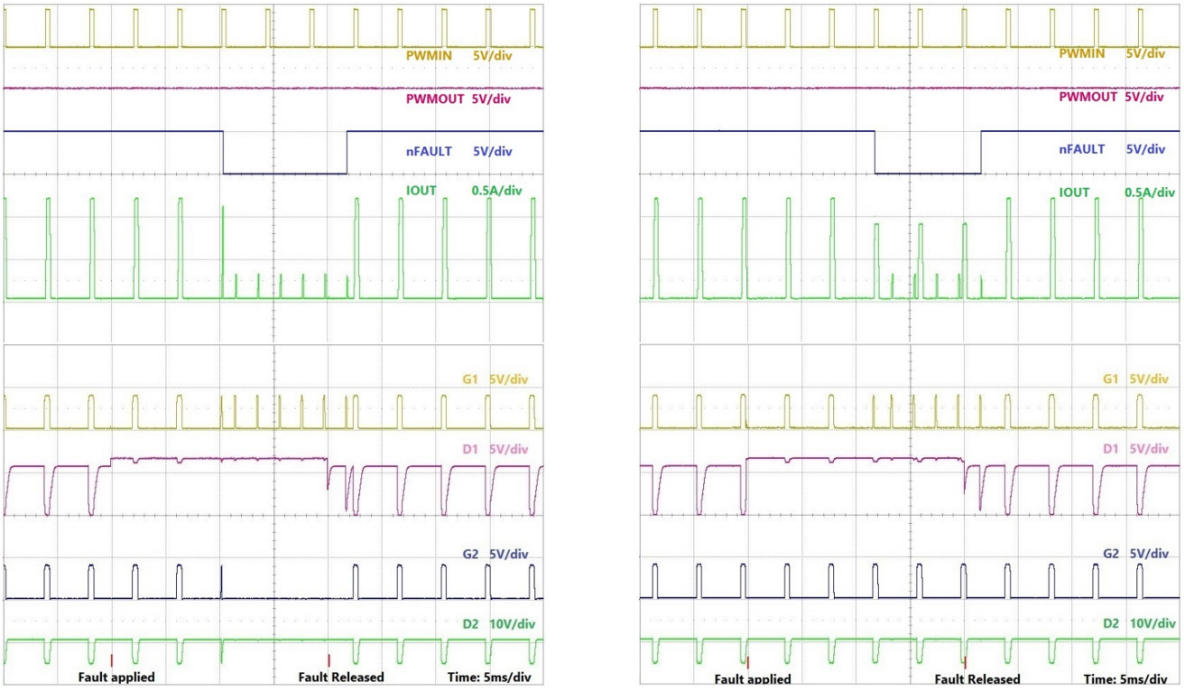

Figure 16: Drain Short to VIN Fault on D1 with External PWM Dimming. MODE = High (left), MODE = Low (right).

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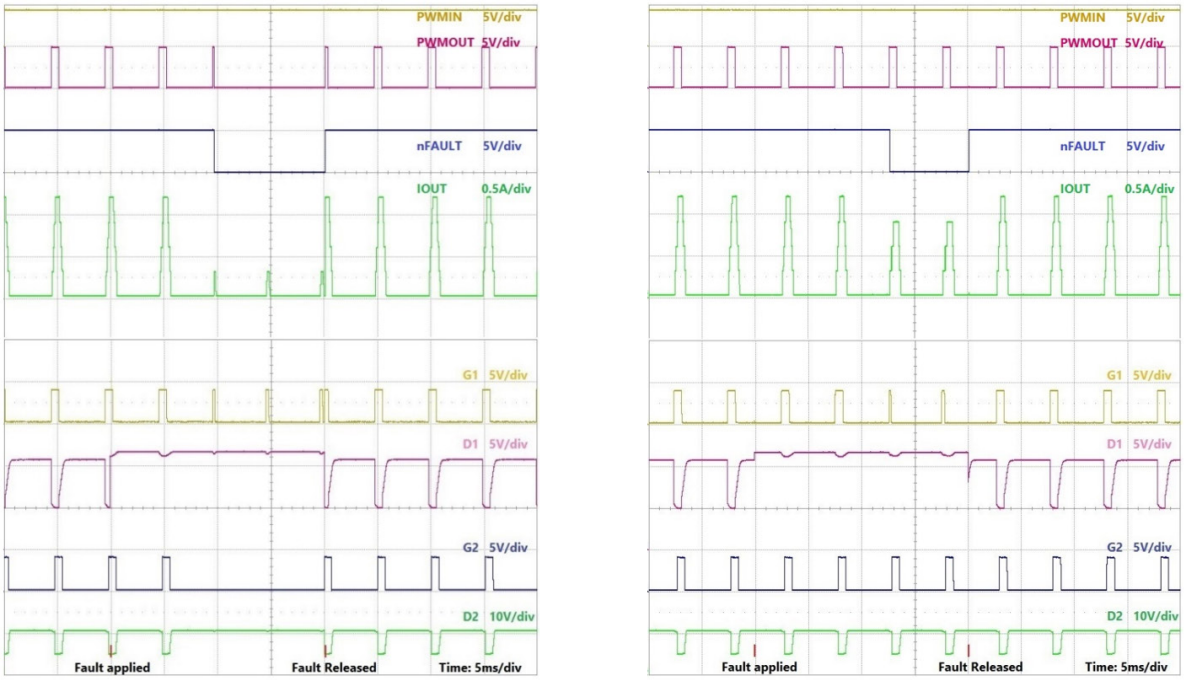

Figure 17: Drain Short to VIN Fault on D1 with Internal PWM Dimming. MODE = High (left), MODE = Low (right).

LED Short Response

If less than the full LED string is shorted, the A80804 continues to work normally. This will lead to increased power dissipation in the LED string's MOSFET.

Input Undervoltage Protection

When input voltage, V_{IN}, is below the undervoltage lockout threshold defined by five times the voltage on the UVLO pin, $V_{IN} < 5 \times V_{UVLO}$, an input undervoltage fault is detected. If MODE is high while an undervoltage fault occurs, the device is off, and if MODE is low, the device stays on. The fault flag nFAULT is not affected by this fault.

Input Overvoltage Derating

The A80804 can derate the LED current at higher input voltages to limit the power dissipation in the MOSFETs. The input voltage level to start derating, $V_{INth(L)}$, is ten times the voltage at the VINDERAT pin plus 0.7 V, $10 \times V_{VINDERAT} + 0.7$ V, and is typically set with a resistor divider from VBIAS pin to VINDERAT pin. The level for maximum derating, $V_{INth(H)}$ is higher than $V_{INth(L)}$ by V_{INthd} (typically 2.16 V). The reference voltage, V_{SENSE}, decreases to 90% of its nominal value at $V_{INth(L)}$ and to 60% at $V_{INth(H)}$; see Figure 18 and Figure 19. The maximum derating is 50% for higher input voltage levels. See Equation 12 to calculate the voltage at VINDERAT pin for a target $V_{INth(L)}$ level.

Equation 12:

$$V_{VINDERAT} = (V_{INth(L)} - 0.7) / 10$$

For example, when $V_{VINDERAT} = 2.0$ V, V_{SENSE} will derate to 90% of its nominal value when $V_{IN} = 20.7$ V.

Even if the VINDERAT pin is tied to VBIAS, the A80804 will begin derating the LED current at 35 V (typical).

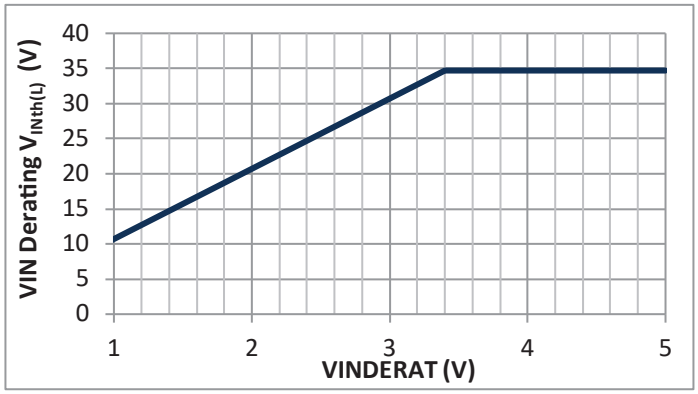

Figure 18: $V_{INDERAT}$ Voltage versus V_{IN} Derating Threshold

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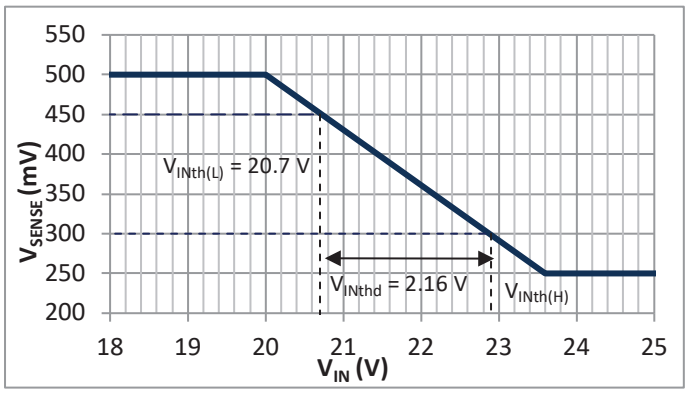

Figure 19: Output Current Foldback Based on V_{IN}

Thermal Derating and Protection Shutdown

At higher temperatures, the A80804 will derate the LED current to limit power dissipation in the external MOSFETs. The reference voltage, V_{SENSE}, decreases with increasing T_J as shown in Figure 20, where V_{SENSE} derates to 90% at 149°C (typical) and 35% at 163°C (typical). The maximum thermal derating is 25% of the nominal current. Thermal shutdown (T_{SD}) completely disables the outputs under extreme overtemperature conditions (>170°C), and nFAULT goes low. The A80804 restarts when the temperature drops by 30°C.

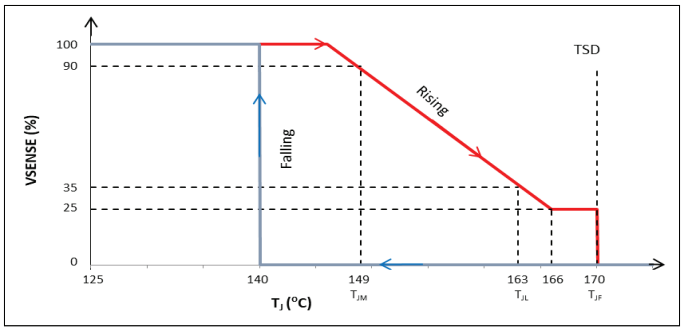

Figure 20: Output Current Foldback Based on Rising T_J

The combined effect of V_{IN} and thermal derating is shown in Figure 21.

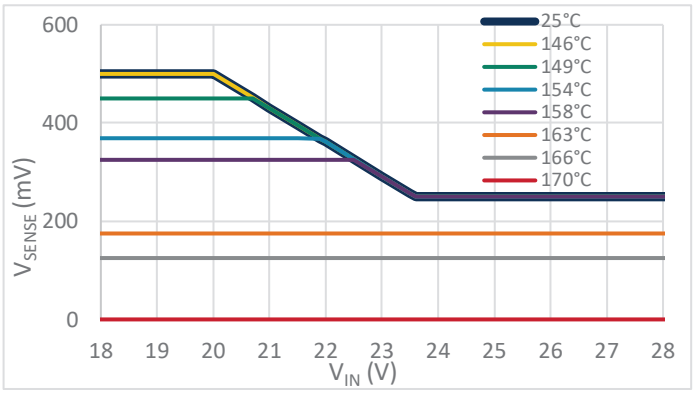

Figure 21: Combined Effect of V_{IN} Derating and Thermal Derating

LED peak current also depends on voltage on ADIMx pin even during V_{IN} and thermal derating.

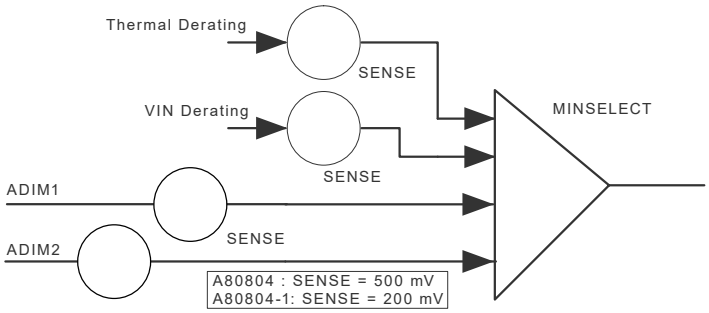

Figure 22: Analog Dimming and Derating Block Diagram

Shutdown

While operating in internal PWM mode, each LED channel resets when its corresponding PWMINx pin is pulled low. While operating in external PWM mode, each LED channel resets when its corresponding PWMINx pin is pulled low for more than 20 ms.

When a channel is reset, its corresponding gate is pulled low and any faults associated with that channel are reset. The rest of the device operates normally. If a faulty string is disabled by pulling PWMINx pin low for greater than 20 ms, the device returns to normal operation for remaining channels and nFAULT is released.

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Table 1: Fault Operation and Derating (Internal PWM mode)

	nFAULT	MODE = VBIAS		MODE = Low	
		PWMOUT	Operation	PWMOUT	Operation
Drain Shorted to VIN	Low	Low	Detected for three consecutive PWM cycles when (V_{IN} – V_{Dx}) < 0.8 V. The faulty MOSFET remains on with 5% PWM. Other strings, PWMOUT, and nFAULT pulled low once fault detected. The fault is not latched. The faulty MOSFET will drop the full input voltage during PWM on-time. The device recovers to normal operation when the fault is removed.	Normal	Detected for three consecutive PWM cycles when (V_{IN} – V_{Dx}) < 0.8 V. The faulty MOSFET remains on with 5% PWM, rest of IC operates normally except nFAULT pin is pulled low. The faulty MOSFET drop full input voltage during PWM on-time. The device recovers to normal operation when the fault is removed.
	The fault is detected when corresponding PWMIN pin is high and the configured slew time has elapsed.				
Open LED	Low	Low	Detected for three consecutive PWM cycles when V_{IN} > 5 × V_{FDIS} and V_{Dx} < 0.24 V. The faulty MOSFET remains on with 5% PWM. Other strings, PWMOUT, and nFAULT pulled low once fault detected. The fault is not latched. The device recovers to normal operation when fault removed.	Normal	Detected for three consecutive PWM cycles when V_{IN} > V_{FDIS} and V_{Dx} < 0.24 V. The faulty MOSFET remains on with 5% PWM, rest of the device operates normally except nFAULT pin is pulled low. nFAULT pin goes high when the fault is removed.
Drain Shorted to GND	Low	Low	Detected for three consecutive PWM cycles when V_{IN} > 5 × V_{FDIS} and V_{Dx} < 0.24 V. The faulty string remains on with 5% PWM. Other strings, PWMOUT, and nFAULT pulled low once fault detected. The fault is not latched. The device recovers to normal operation when fault removed. LEDs in faulty string may be damaged due to excessive LED current.	Normal	Detected for three consecutive PWM cycles when V_{IN} > V_{FDIS} and V_{Dx} < 0.24 V. The faulty string remains on with 5% PWM, rest of the device operates normally except nFAULT pin is pulled low LEDs in faulty string may damage due to excessive LED current. The nFAULT pin goes high when the fault is removed.
Thermal Derating	Normal	Normal	LED current derates based on junction temperature.	Same operation as MODE = VBIAS	
VIN Derating	Normal	Normal	LED current derates based on supply voltage and VINDERAT setting.	Same operation as MODE = VBIAS	
TSD	Low	Low	LEDs turn off when T_J exceeds 170°C and auto-recovers when T_J drops below 140°C.	Normal	LEDs turn off when T_J exceeds 170°C but PWMOUT is normal. The device auto-recovers when T_J drops below 140°C.
VIN Undervoltage	Normal	Low	LEDs turn off when V_{IN} < V_{INUV} – $V_{INUVhys}$ and auto-restart when V_{IN} rises above V_{INUV}.	Normal	A80804 operates normally. LED current may reduce if V_{IN} < V_F. nFAULT is not affected.

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Table 2: Fault Operation and Derating (External PWM mode)

	nFAULT	MODE = VBIAS		MODE = Low	
		PWMOUT	Operation	PWMOUT	Operation
Drain Shorted to VIN	Low	Low	Detected for three consecutive PWM cycles when (V_{IN} – V_{Dx}) < 0.8 V. The faulty string remains on with 5%, 500 Hz PWM. Other strings, PWMOUT, and nFAULT pulled low once fault detected. Faulty MOSFET drops full VIN voltage during PWM. IC recovers to normal operation when fault removed.	Low	Detected for three consecutive PWM cycles when (V_{IN} – V_{Dx}) < 0.8 V. The faulty string remains on with 5%, 500 Hz PWM. Rest of the IC operates normally except nFAULT pin pulled low. Faulty MOSFET drops full VIN voltage during PWM IC recovers to normal operation when fault removed.
	The fault is detected when all PWMIN high and after completion of reference ramp.				
Open LED	Low	Low	Detected for three consecutive PWM cycles when V_{IN} > 5 × V_{FDIS} and V_{Dx} < 0.24 V. The faulty string remains on with 5%, 500 Hz PWM. Other strings, PWMOUT, and nFAULT pulled low once fault detected. IC recovers to normal operation when fault removed.	Low	Detected for three consecutive PWM cycles when V_{IN} > V_{FDIS} and V_{Dx} < 0.24 V. The faulty string remains on with 5%, 500 Hz PWM, rest of IC operates normally except nFAULT pin pulled low. nFAULT pin goes high when fault removed.
Drain Shorted to GND	Low	Low	Detected for three consecutive PWM cycles when V_{IN} > 5 × V_{FDIS} and V_{Dx} < 0.24 V. The faulty string remains on with 5%, 500 Hz PWM. Other strings, PWMOUT, and nFAULT pulled low once fault detected. IC recovers to normal operation when fault removed. LEDs in faulty string may damage due to excessive LED current.	Low	Detected for three consecutive PWM cycles when V_{IN} > V_{FDIS} and V_{Dx} < 0.24 V. The faulty string remains on with 5%, 500 Hz PWM, rest of IC operates normally except nFAULT pin pulled low. nFAULT pin goes high when fault removed. LEDs in faulty string may damage due to excessive LED current.

VIN derating, Thermal derating, TSD, and VIN undervoltage fault operation is same as described in Table 1.

Table 3: Fault Operation and Derating (FULL mode)

	nFAULT	MODE = VBIAS		MODE = Low	
		PWMOUT	Operation	PWMOUT	Operation
Drain Shorted to VIN	Low	Low	Detected when (V_{IN} – V_{Dx}) < 0.8 V for 6 ms. The faulty string remains on with 5%, 500 Hz PWM. Other strings, PWMOUT, and nFAULT pulled low once fault detected but not latched. Faulty MOSFET drop full VIN voltage during PWM. IC recovers to normal operation when fault removed.	Normal	Detected when (V_{IN} – V_{Dx}) < 0.8 V for 6 ms. The faulty string remains on with 5%, 500 Hz PWM, rest of IC operates normally except nFAULT pin pulled low. Faulty MOSFET drop full VIN voltage during PWM. IC recovers to normal operation when fault removed.
	The fault is detected when all PWMIN high and after completion of reference ramp.				
Open LED	Low	Low	Detected when V_{IN} > 5 × V_{FDIS} and V_{Dx} < 0.24 V for 6 ms. The faulty string remains on with 5%, 500 Hz PWM. Other strings, PWMOUT, and nFAULT pulled low once fault detected but not latched. IC recovers to normal operation when fault removed.	Normal	Detected when V_{IN} > V_{FDIS} and V_{Dx} < 0.24 V for 6 ms. The faulty string remains on with 5%, 500 Hz PWM, rest of IC operates normally except nFAULT pin pulled low. nFAULT pin goes high when fault removed.
Drain Shorted to GND	Low	Low	Detected when V_{IN} > 5 × V_{FDIS} and V_{Dx} < 0.24 V for 6 ms. The faulty string remains on with 500 Hz, 5% PWM. Other strings, PWMOUT, and nFAULT pulled low once fault detected but not latched. IC recovers to normal operation when fault removed LEDs in faulty string may damage due to excessive LED current.	Normal	Detected when V_{IN} > V_{FDIS} and V_{Dx} < 0.24 V for 6 ms. The faulty string remains on with 500 Hz, 5% PWM, rest of IC operates normally except nFAULT pin pulled low LEDs in faulty string may damage due to excessive LED current. nFAULT pin goes high when fault removed.

VIN derating, Thermal derating, TSD, and VIN undervoltage fault operation is same as described in Table 1.

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Table 4: Simplified Fault Table

Description	Detection Condition	FULL	MODE = HIGH				MODE = LOW			
			nFAULT	Faulty Gate	NORMAL Gates	PWM_ OUT [3]	nFAULT	Faulty Gate	NORMAL Gates	PWM_ OUT [3]
Drain Shorted to VIN [1]	$V_{IN} - V_{Dx}$ < typ 0.8 V (min 0.5 V, max 1.1 V)	HIGH	LOW	5% PWM	LOW	LOW	LOW	5% PWM	HIGH	HIGH
		LOW	LOW	5% PWM	LOW	LOW	LOW	5% PWM	PWM	PWM
Open LED Fault [2]	V_{Dx} < typ 0.24 V (min 0.19 V, max 0.29 V)	HIGH	LOW	5% PWM	LOW	LOW	LOW	5% PWM	HIGH	HIGH
		LOW	LOW	5% PWM	LOW	LOW	LOW	5% PWM	PWM	PWM
Drain Shorted to GND [2]	V_{Dx} < typ 0.24 V (min 0.19 V, max 0.29 V)	HIGH	LOW	5% PWM	LOW	LOW	LOW	5% PWM	HIGH	HIGH
		LOW	LOW	5% PWM	LOW	LOW	LOW	5% PWM	PWM	PWM
Thermal Shutdown	T_J > 170°C	X	LOW	LOW	LOW	LOW	LOW	LOW	LOW	Normal

X = Don't Care
[1] Detected after completion of slew time.
[2] $V_{IN} > 5 \times V_{FDIS}$.
[3] Applicable only for FULL and internal PWM mode.

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APPLICATIONS INFORMATION

MOSFET Selection Guidelines

The A80804 uses N-channel MOSFETs for controlling the LED current. The following should be considered when selecting a MOSFET:

- Drain-source voltage must be higher than the maximum input voltage.
- Drain current rating must be higher than LED current.
- For low voltage operation (V_{IN} < 7 V), select a logic level MOSFET.
- The MOSFETs power dissipation is at the worst-case condition in FULL mode at max V_{IN}, based on Equation 13.

  Equation 13:

$$P_D = (V_{IN(max)} - V_{Fmin}) \times I_{LED}$$

- Select MOSFET to handle the power without exceeding junction temperature rating, T_J, of the MOSFET. A proper PCB layout is recommended to minimize temperature rise.
- MOSFET input capacitance, C_{iss} should be 250 pF < C_{iss} < 2000 pF.
- MOSFETs can be paralleled with above considerations.

Some recommended MOSFETs are given below in Table 5.

Table 5: Sample of Possible MOSFETs

Max. Input Voltage = 40 V					
Part Number	**V_{DS} (V)**	**I_D (A)**	**Package**	**C_{iss} (pF)**	**Application**
BUK7M67-60E	60	14	LFPAK33	250	I_{LED} < 300 mA, V_{IN} > 7 V
RD3L080S	60	8	DPAK	380	I_{LED} < 700 mA
NVD5867NL	60	22	DPAK	675	I_{LED} < 700 mA
BUK7675-55A	55	20.3	D2PAK	320	I_{LED} > 700 mA

Note: These MOSFETs are only for guidance, actual selection will depend on application requirements and required power dissipation (thermal design).

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Four 2-LED Channels, Internal PWM at 200 Hz, 5% Duty Cycle, Without Analog Dimming

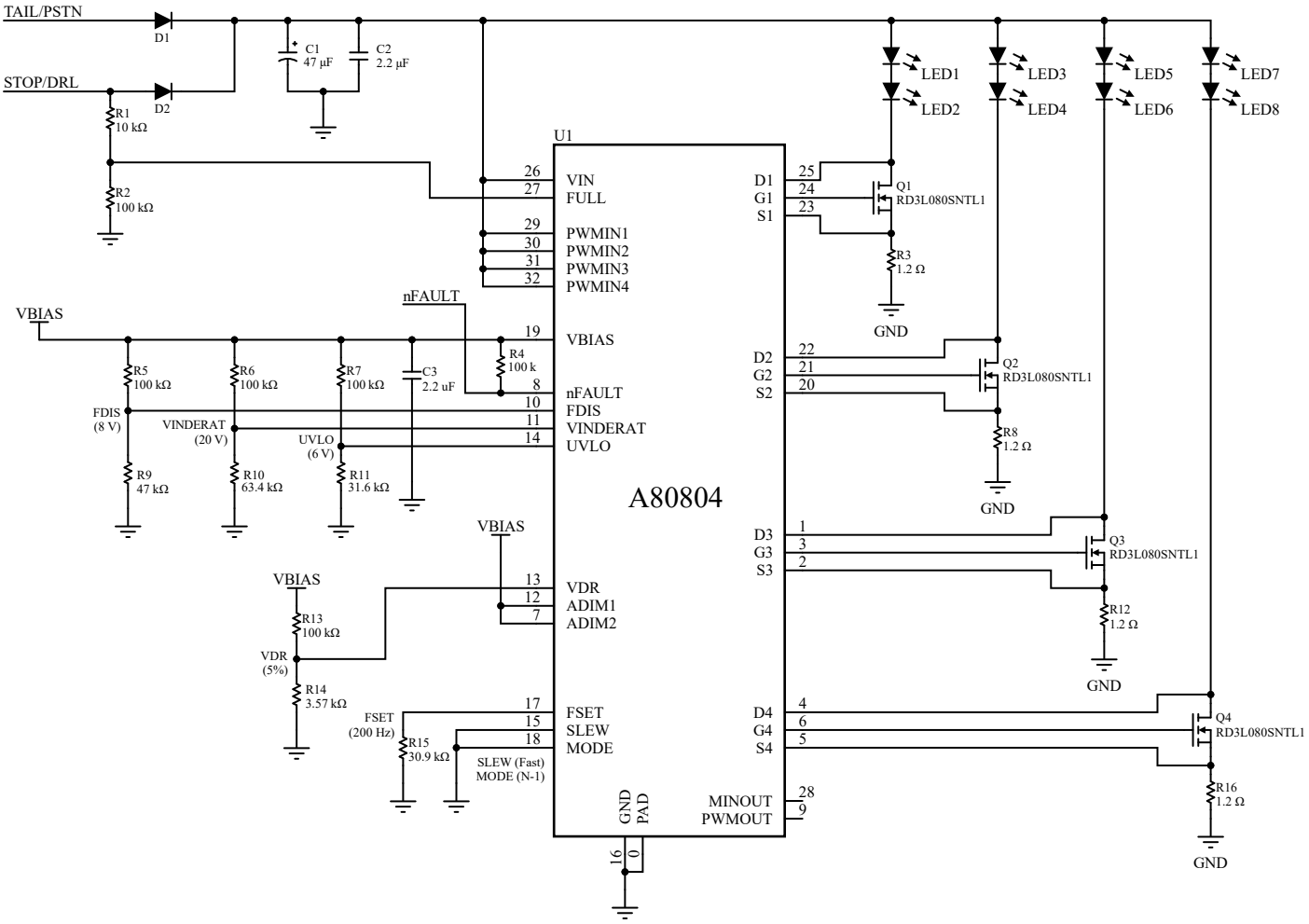

Figure 23: Application Circuit for Four 2-LED Channels, Internal PWM at 200 Hz, 5% Duty Cycle, Without Analog Dimming

Design Requirements

Requirement	Value	Unit
$V_{IN(MIN)}$ (UVLO)	6	V
$V_{IN(MIN)}$ (regulation)	8	V
$V_{F(max)}$	6.4	V
I_{LED}	400	mA
f_{PWM}	200	Hz
Duty Cycle (D)	5	%
V_{IN} Derate Start	20	V
No analog dimming	–	–

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Bill of Materials

Designator	Description	Quantity
C1	Capacitor, Electrolytic, 47 µF, 50 V, 10%	1
C2	Capacitor, Ceramic, 2.2 µF, 50 V, 10%, X7R	1
C3	Capacitor, Ceramic, 2.2 µF, 16 V, 10%, X7R	1
D1, D2	Diode	2
LED1, LED2, LED3, LED4, LED5, LED6, LED7, LED8	LED 3 V	8
Q1, Q2, Q3, Q4	MOSFET N-CH 60 V 8 A TO-252-2 (DPAK)	4
R1, R2, R4, R5, R6, R7, R13	Resistor, 100 kΩ, 1/8 W, 1 %, 0603	7
R3, R8, R12, R16	Resistor, 1.2 Ω, 1/2 W, 1 %, 1206	4
R9	Resistor, 47 kΩ, 1/8 W, 1 %, 0603	1
R10	Resistor, 63.4 kΩ, 1/8 W, 1 %, 0603	1
R11	Resistor, 31.6 kΩ, 1/8 W, 1 %, 0603	1
R14	Resistor, 3.57 kΩ, 1/8 W, 1 %, 0603	1
R15	Resistor, 30.9 kΩ, 1/8 W, 1 %,0603	1
U1	A80804 in QFN-32	1

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Four 2-LED Channels, External PWM, Analog Dimming at 80%

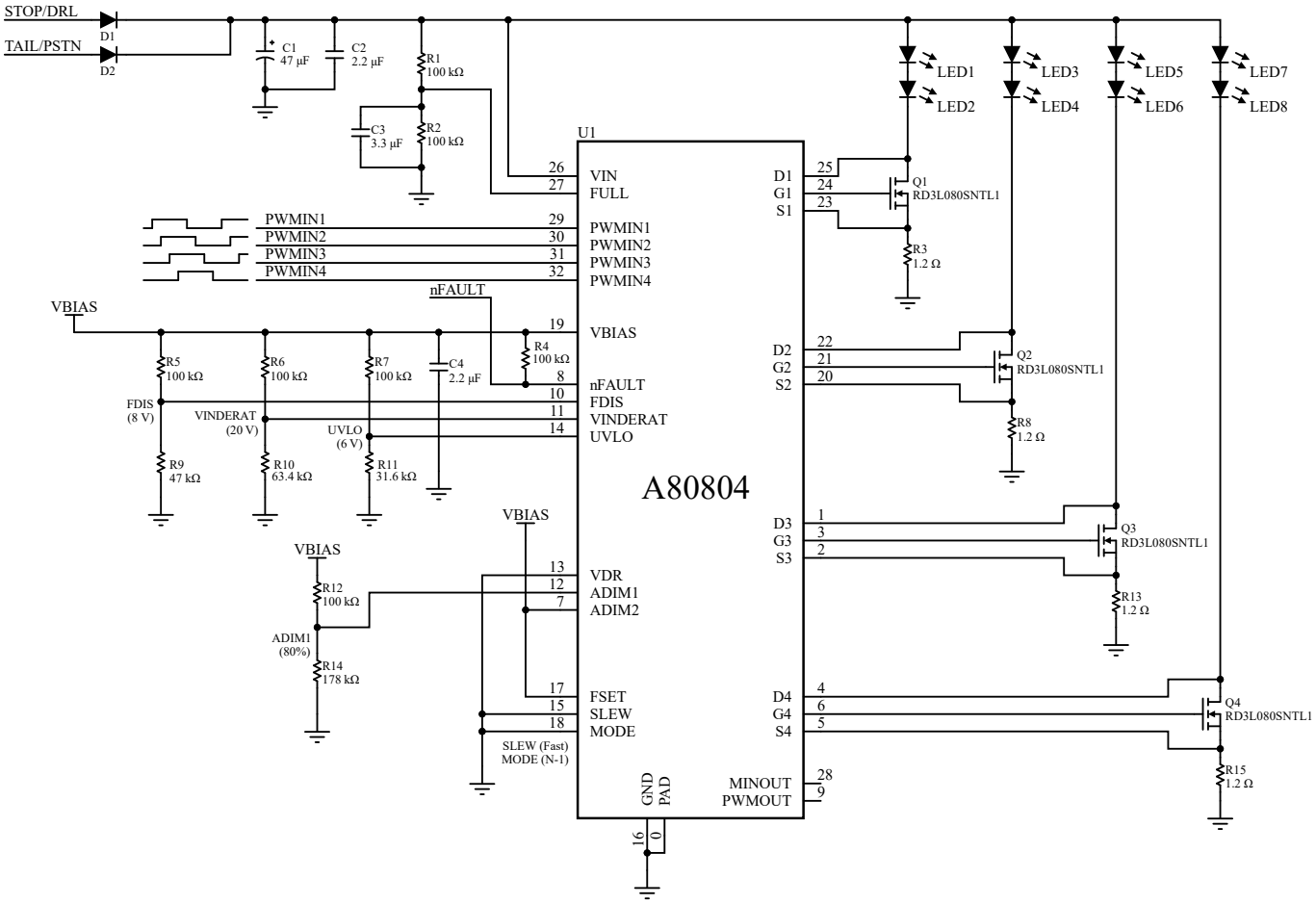

Figure 24: Application Circuit for Four 2-LED Channels, External PWM, Analog Dimming at 80%

Design Requirements

Requirement	Value	Unit
$V_{IN(MIN)}$ (UVLO)	6	V
$V_{IN(MIN)}$ (regulation)	8	V
$V_{F(max)}$	6.4	V
I_{LED}	400	mA
f_{PWM}	External	Hz
Duty Cycle (D)	External	%
V_{IN} Derate Start	20	V
ADIM1	80	%

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Bill of Materials

Designator	Description	Quantity
C1	Capacitor, Electrolytic, 47 µF, 50 V, 10%	1
C2	Capacitor, Ceramic, 2.2 µF, 50 V, 10%, X7R	1
C3	Capacitor, Ceramic, 3.3 µF, 50 V, 10%, X7R	1
C4	Capacitor, Ceramic, 2.2 µF, 16 V, 10%, X7R	1
D1, D2	Diode	2
LED1, LED2, LED3, LED4, LED5, LED6, LED7, LED8	LED 3 V	8
Q1, Q2, Q3, Q4	MOSFET N-CH 60 V 8 A TO-252-2 (DPAK)	4
R1, R2, R4, R5, R6, R7, R12	Resistor, 100 kΩ, 1/8 W, 1 %, 0603	7
R3, R8, R13, R15	Resistor, 1.2 Ω, 1/2 W, 1 %, 1206	4
R9	Resistor, 47 kΩ, 1/8 W, 1 %, 0603	1
R10	Resistor, 63.4 kΩ, 1/8 W, 1 %, 0603	1
R11	Resistor, 31.6 kΩ, 1/8 W, 1 %, 0603	1
R14	Resistor, 178 kΩ, 1/8 W, 1 %, 0603	1
U1	A80804 in QFN-32	1

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Multiple A80804 Master-Slave Arrangement

The master IC is configured as a single IC in Internal PWM mode. In TAIL mode, a resistor on the FSET pin determines the PWM frequency, and the duty cycle is controlled by voltage on the VDR pin. In Full mode, duty cycle is always 100%.

Operating PWM frequency and duty cycle output is provided on the PWMOUT pin. Connect this pin to the PWMINx pins of the slave ICs. Each slave IC is configured in external PWM mode.

Master and slaves derate LED current independently, based on VIN pin voltage and junction temperature of the respective device. Overtemperature or input overvoltage conditions derate LED current by controlling peak current in both Stop and Tail modes.

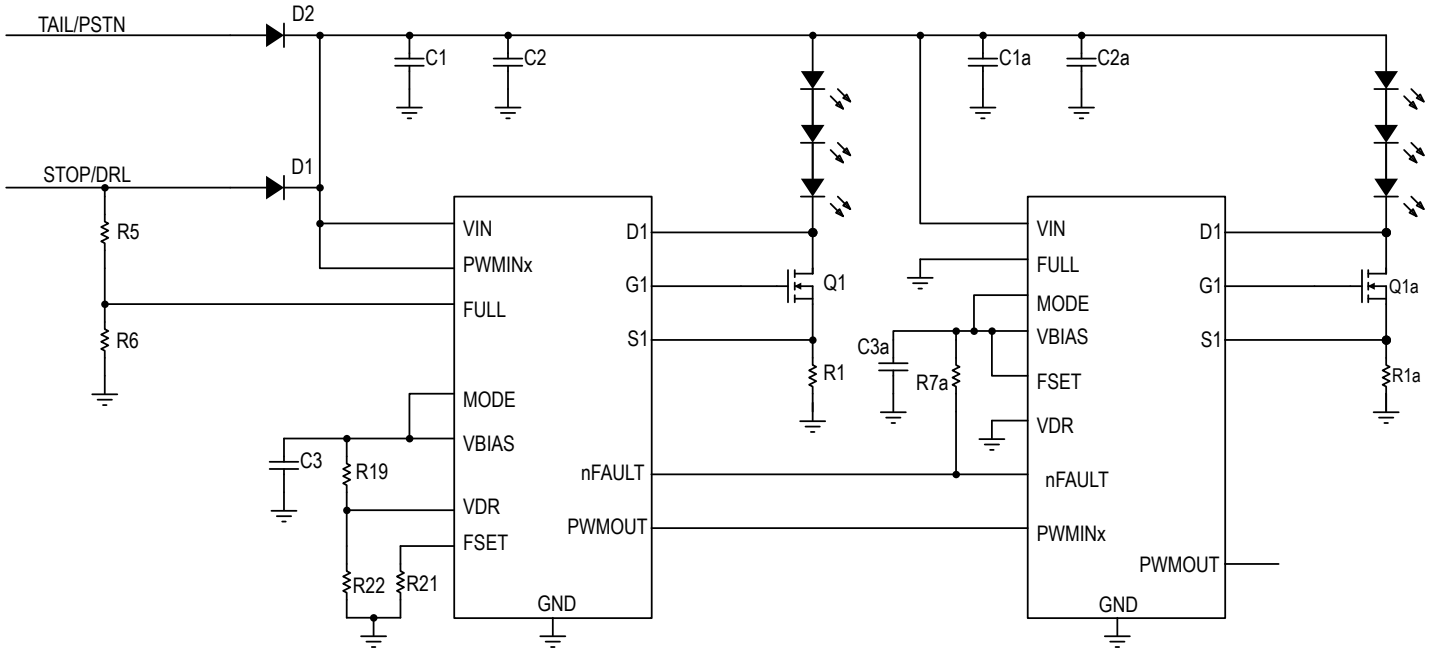

Figure 25: Master-Slave Operation with Internal PWM. Only one channel shown for simplicity.

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Multiple A80804 In Parallel with External Dimming

All the A80084 devices are configured for external PWM mode. PWM input from the MCU controls frequency and duty cycle in Tail mode. In Stop mode, duty cycle is always 100%.

Each IC derates LED current independently, based on VIN pin voltage and junction temperature of the respective IC.

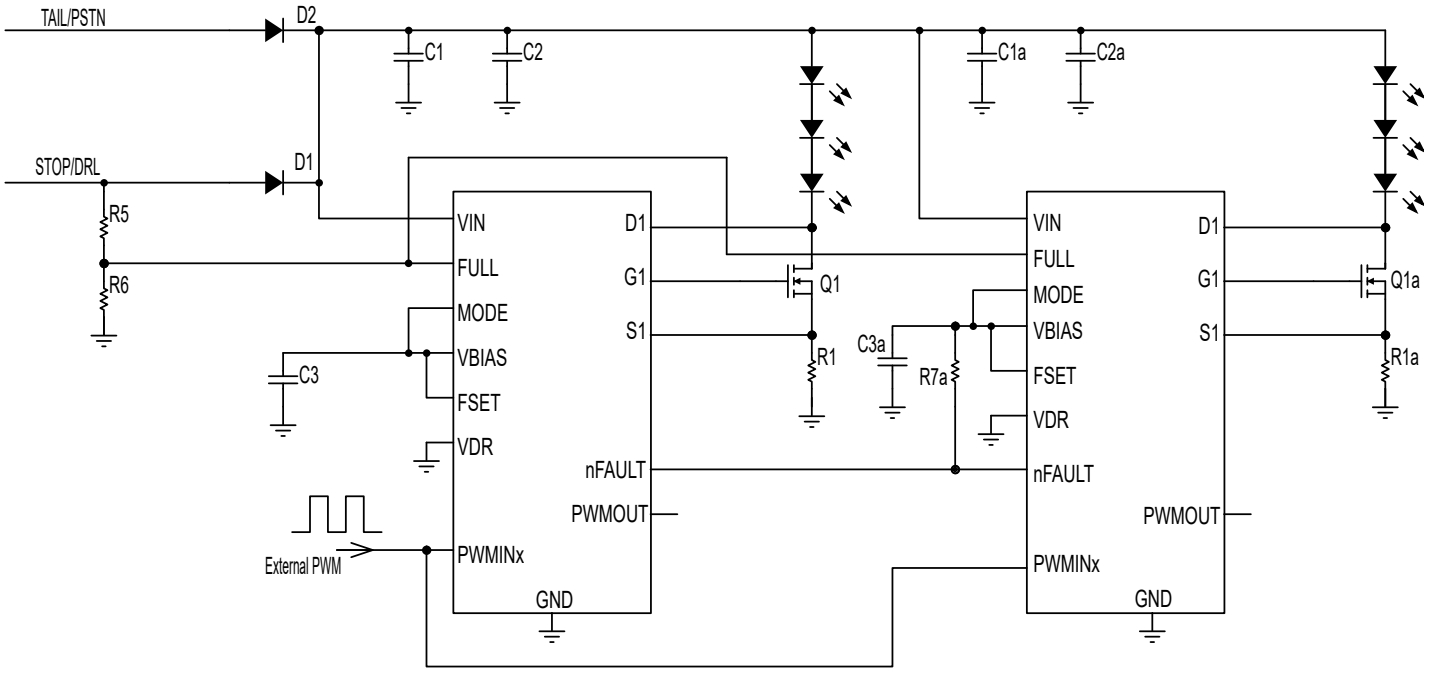

Figure 26: Parallel Operation with External PWM. Only one channel shown for simplicity.

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Sequential LED Driver

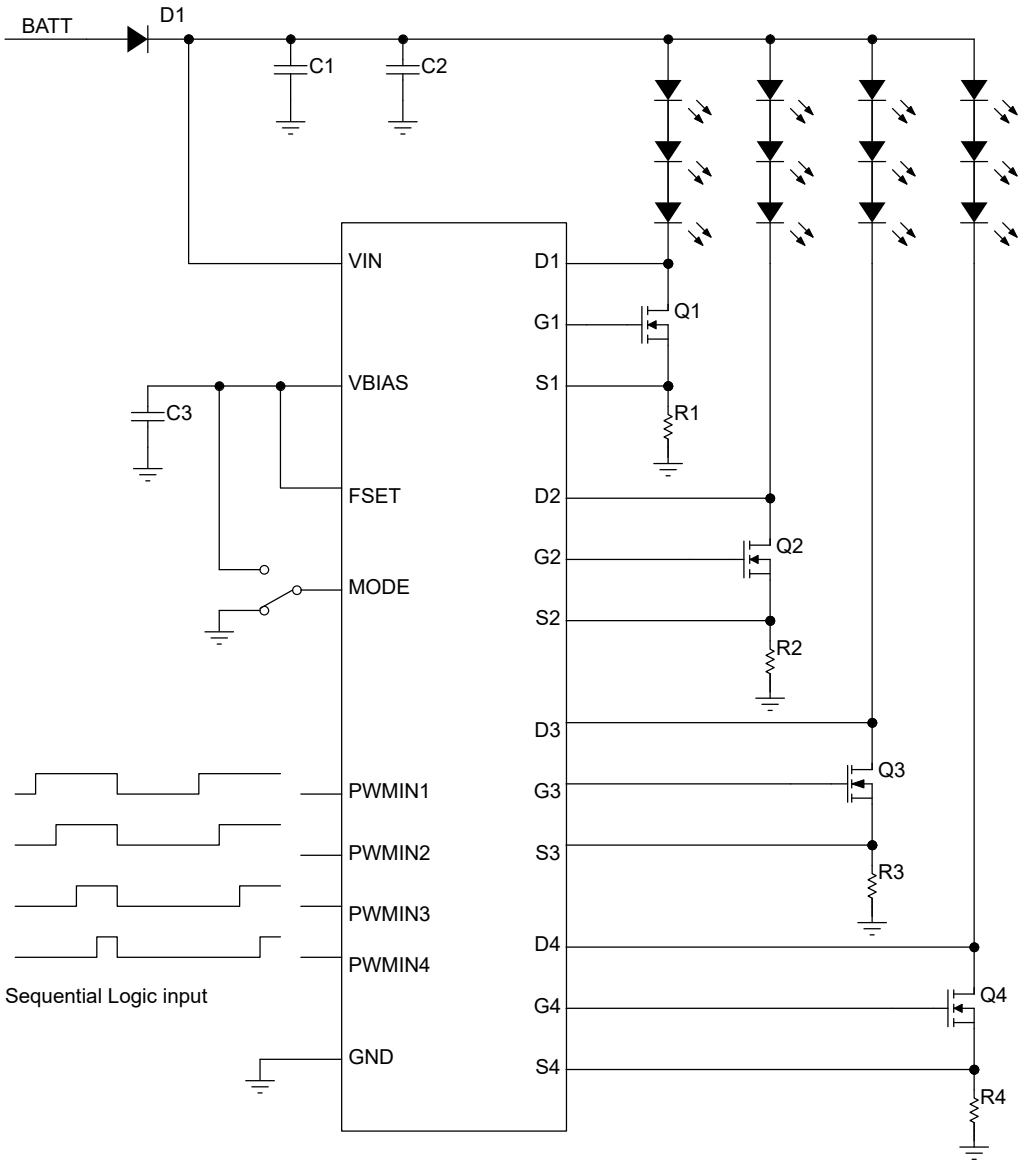

Figure 27: Sequential LED driver
Each sequence is about 50-200 ms and off period could be up to 0.6 seconds.
Faults will reset in each cycle as off period is > 20 ms.

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LED Binning and NTC Derating

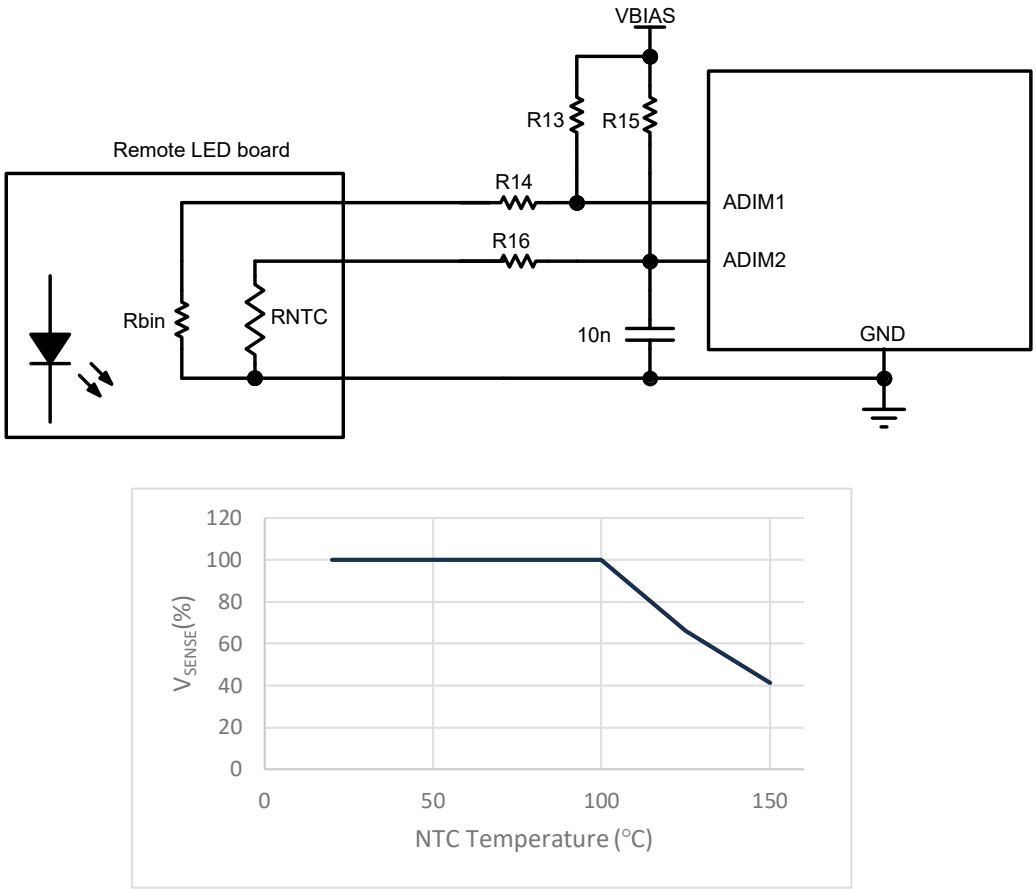

Figure 28: Typical External Thermal Derating and Binning Arrangement

A capacitor across ADIM1 can be used to avoid noise interference. Thermal derating with NTC (NTCS0805E3104XT) on remote board. The NTC thermistor and binning resistor RBIN can be placed up to 30 cm away from the IC.

Table 6: NTC Characteristic and Thermal Dimming

Temperature (°C)	RNTC (Ω)	R (Ω)	VADIM2 (V)	VSENSE (V)
20	125811	6200	0.953	0.500
25	100000	6200	0.942	0.500
50	34897	6200	0.849	0.500
70	16601	6200	0.728	0.500
85	9988	6200	0.617	0.500
98	6300	6200	0.504	0.500
100	6236	6200	0.501	0.500
125	3055	6200	0.330	0.330
150	1610	6200	0.206	0.206

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Parallel MOSFET Arrangement for High-Power Application

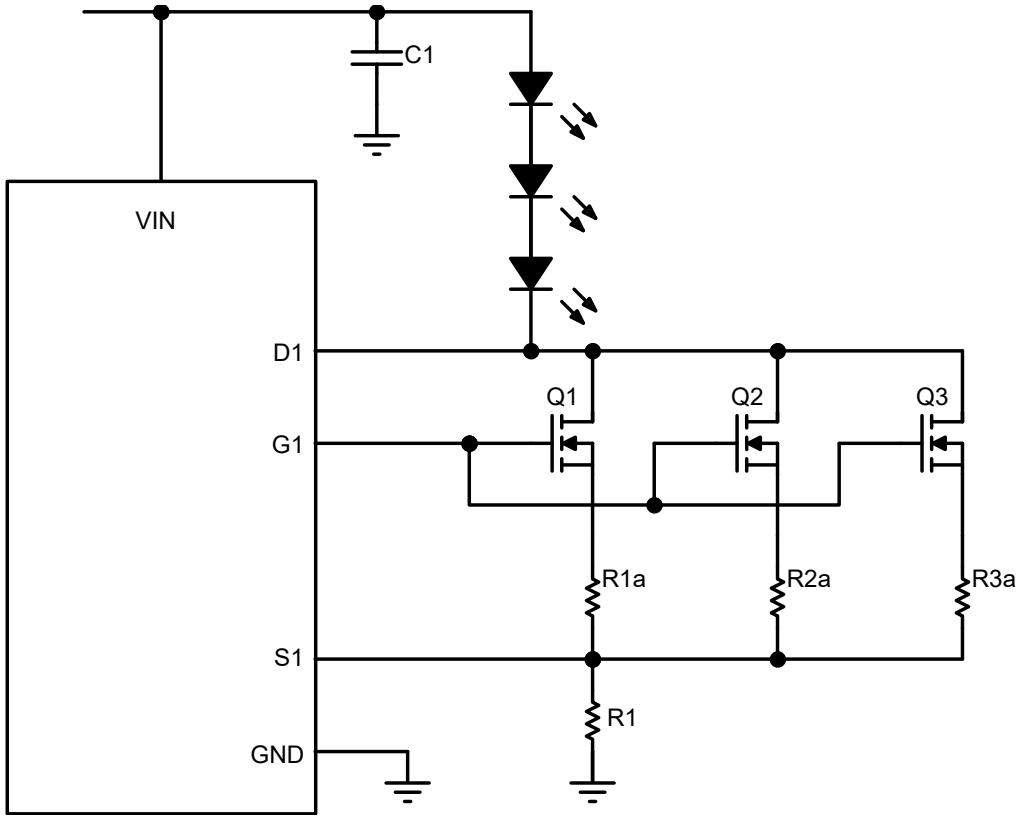

Figure 29: Parallel MOSFET Arrangement for High Power Application

R1a, R2a, and R3a helps in balancing current through MOSFET. Typically for 0.3 A select 1 Ω resistor. Total input capacitance of MOSFETs should be as specified by C_{iss} requirement in MOSFET Selection Guidelines.

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Arrangement to Avoid LED Current in External PWM Mode with Full Pin Connected to VIN and PWMINx Held Low at Startup

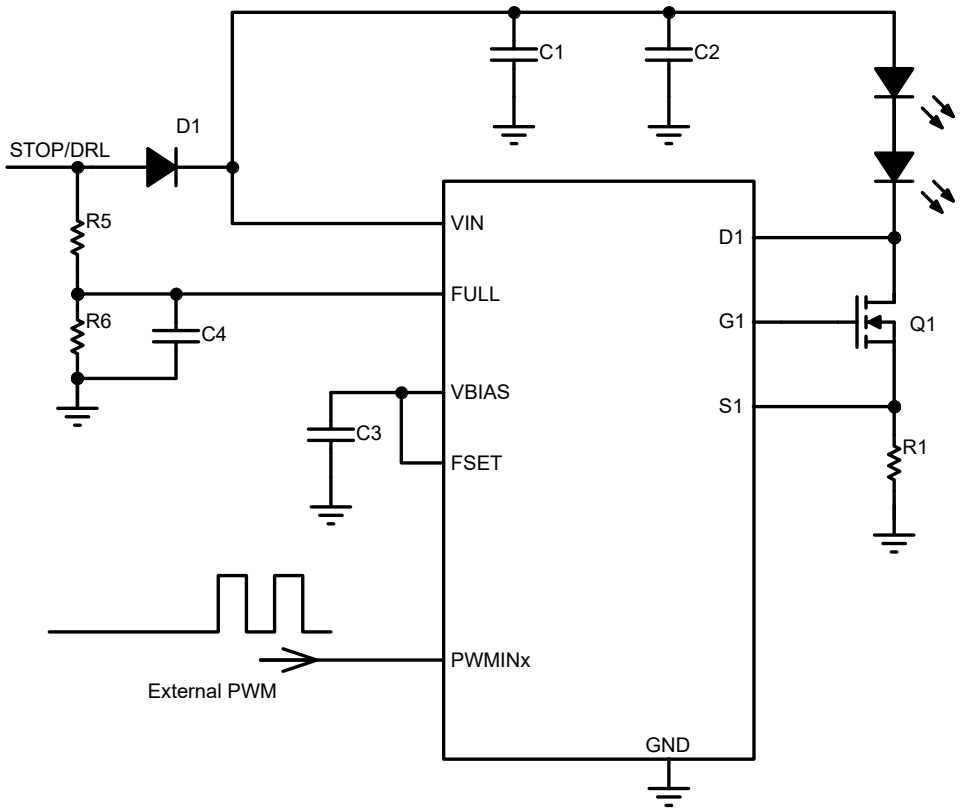

Figure 30: Application to avoid initial LED current in external PWM mode with FULL pin connected to VIN and PWMINx held low at startup.

Design R5-R6 and C4 network to limit voltage on the FULL pin to below 1 V within 20 ms from startup.

If the FULL pin is driven externally such as through a microcontroller, provide a 20 ms delay from startup on the FULL pin.

This delay is not required for internal PWM with FSET connected to GND through frequency setting resistor. This is also not needed if the FULL pin will remain low.

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Quick Summary of Operation

1. Internal PWM mode is selected when the FSET pin is connected to GND through a frequency setting resistor.
2. External PWM mode is selected when the FSET pin is connected to VBIAS.
3. Full mode is selected when the FULL pin is high, and the A80804 operates with 100% duty cycle regardless of internal or external PWM configuration.
4. Individual LED current is set by a current sense resistor from the Sx pin to GND for each channel. This current can be derated with analog dimming.
5. The voltage on each ADIMx pin sets the peak LED current. Analog dimming for each ADIMx pin is disabled if the ADIMx pin is connected to VBIAS.
6. Input voltage derating reduces LED current, similar to analog dimming, when $V_{IN} > 10 \times V_{INDERAT} + 0.7$ V or $V_{IN} > 35$ V.
7. Internal thermal derating reduces LED current when the A80804 experiences high junction temperatures.
8. Open LED fault is disabled when $V_{IN} < 5 \times V_{FDIS}$, where V_{FDIS} is the voltage on FDIS pin. This voltage is usually set by a voltage divider between VBIAS and GND.
9. Input undervoltage fault threshold is set by $5 \times V_{UVLO}$, where V_{UVLO} is the voltage on the UVLO pin. This voltage is usually set by a voltage divider between VBIAS and GND.
10. Faults are detected only on enabled channels.
11. Faults are only detected when PWMINx is high. During PWM low state the fault state is retained. All four channels can control the nFAULT pin. The nFAULT pin will be released if the faulted LED string's PWMINx pin is pulled low for at least 20 ms, allowing faults on other pins to be detected.
12. All unused channels must have the PWMINx pin held low.
13. Pulling the MODE pin high sets the fault response action to "one-out-all-out", and pulling the MODE pin low sets "one-out-continue (N-1)" mode, where all other LED strings without a fault continue operating. When the MODE pin is high, the nFAULT pin acts as bidirectional fault pin, where multiple A80804 devices can react to a fault together.
14. Faults do not latch; the part will recover when a fault is removed.

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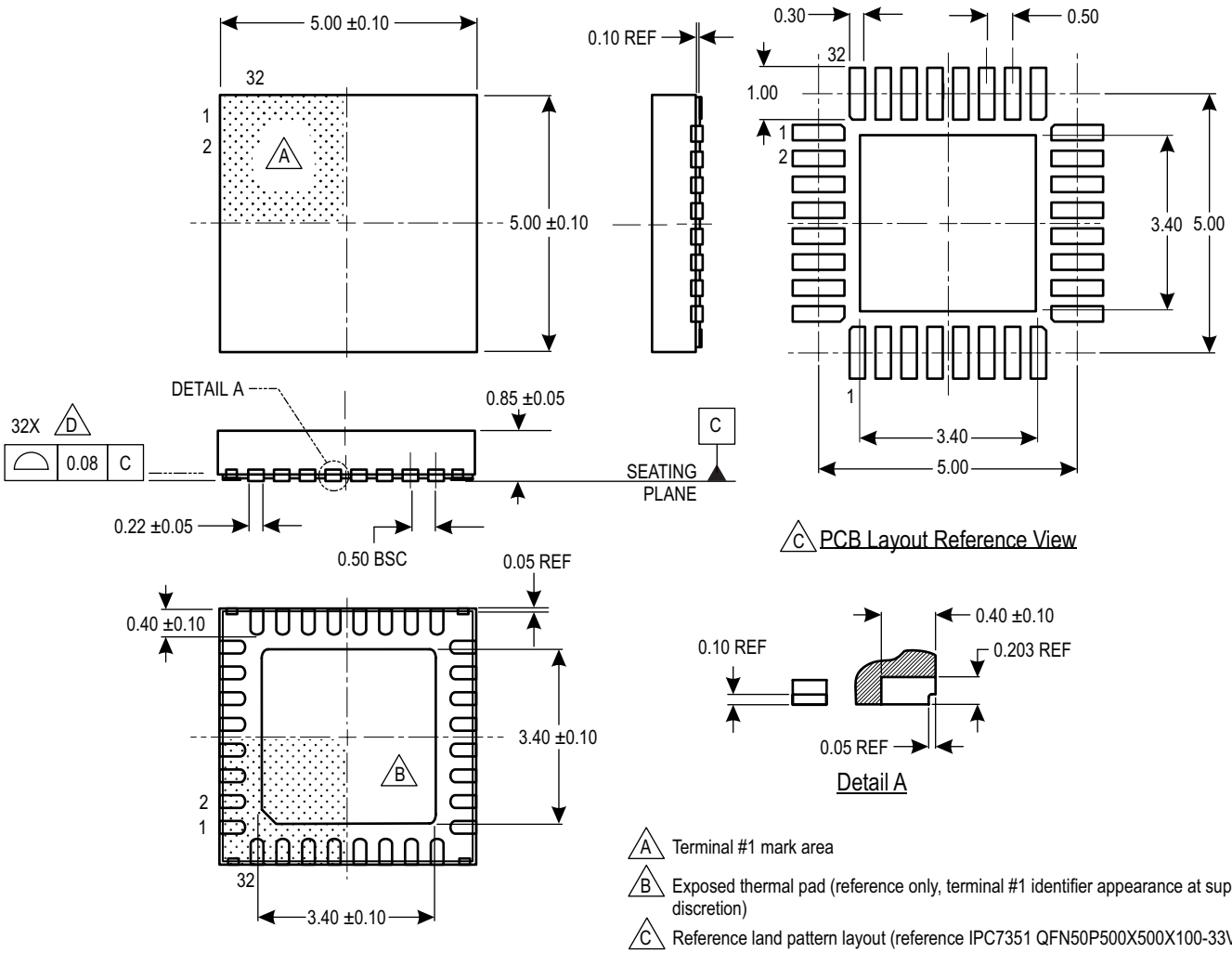
PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference JEDEC MO-220VHHD-6)
Dimensions in millimeters – NOT TO SCALE
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P500X500X100-33V6M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

Figure 31: 32-Pin 5 mm × 5 mm QFN with exposed thermal pad and wettable flank (suffix ET)

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Revision History

Number	Date	Description
–	September 14, 2021	Initial release

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