A1356

High Precision Linear Hall-Effect Sensor IC with Open Drain Pulse Width Modulated Output

Not for New Design

The A1356 is in production but has been determined to be NOT FOR NEW DESIGN. This classification indicates that sale of this device is currently restricted to existing customer applications. The device should not be purchased for new design applications because obsolescence in the near future is probable. Samples are no longer available.

Date of status change: June 22, 2022

Recommended Substitutions:

For existing customer transition, and for new customers or new applications, contact Allegro Sales.

NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

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High Precision Linear Hall-Effect Sensor IC with Open Drain Pulse Width Modulated Output

FEATURES AND BENEFITS

- Simultaneous programming of PWM carrier frequency, quiescent duty cycle, and sensitivity; for system optimization
- Factory-programmed sensitivity temperature coefficient and quiescent duty cycle drift
- Programmability at end-of-line
- Pulse-width modulated (PWM) output provides increased noise immunity compared to an analog output
- Precise recoverability after temperature cycling
- Output duty cycle clamps provide short circuit diagnostic capabilities
- Optional 50% duty cycle calibration test mode at device power up
- Wide ambient temperature range: –40°C to 150°C
- Resistant to mechanical stress
- Advanced chopper stabilization circuits and differential signal path design lead to very low output offset levels
- Proprietary on-chip filters provide high output resolution
- Wide power supply operating range: 4.5 to 18 V

PACKAGE: 3-pin SIP (suffix KB)

Not to scale

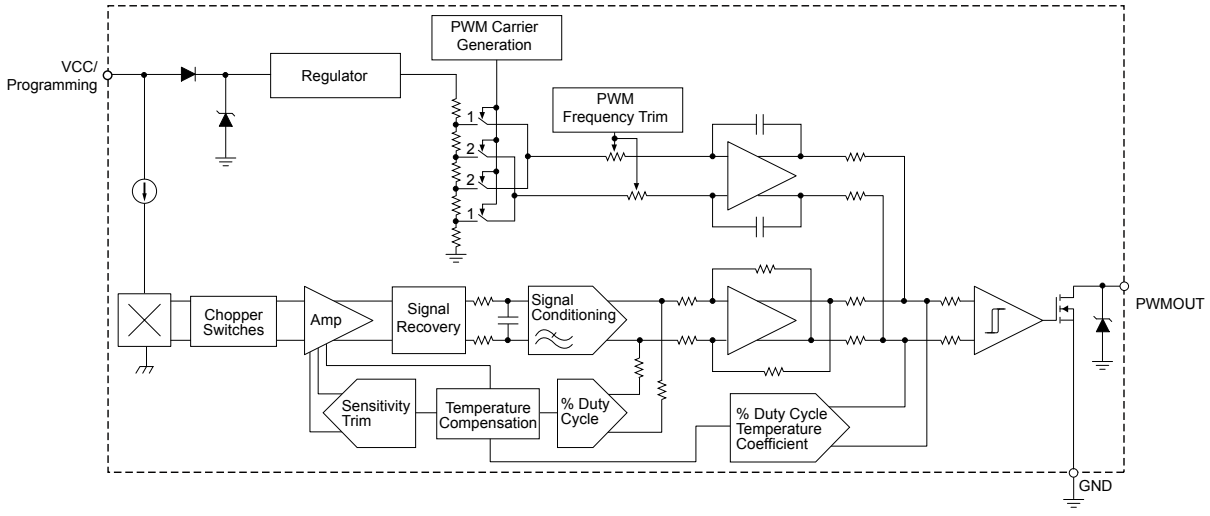
DESCRIPTION

The A1356 device is a high precision, programmable open drain Hall-effect linear sensor IC with a pulse width modulated (PWM) output. The duty cycle (D) of the PWM output signal is proportional to an applied magnetic field. The A1356 device converts an analog signal from its internal Hall element to a digitally encoded PWM output signal. The coupled noise immunity of the digitally encoded PWM output is far superior to the noise immunity of an analog output signal.

The BiCMOS, monolithic circuit inside of the A1356 integrates a Hall element, precision temperature-compensating circuitry to reduce the intrinsic sensitivity and offset drift of the Hall element, a small-signal high-gain amplifier, proprietary dynamic offset cancellation circuits, and PWM conversion circuitry. The dynamic offset cancellation circuits reduce the residual offset voltage of the Hall element. Hall element offset is normally caused by device overmolding, temperature dependencies, and thermal stress. The high frequency offset cancellation (chopping) clock allows for a greater sampling rate, which increases the accuracy of the output signal and results in faster signal processing capability.

The A1356 sensor is provided in a lead (Pb) free 3-pin single inline package (KB suffix), with 100% matte tin leadframe plating.

Functional Block Diagram



SELECTION GUIDE

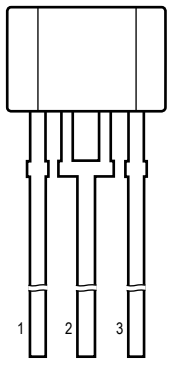
Part Number	Packing*
A1356LKB-T	500 pieces per bag

*Contact Allegro™ for additional packing options

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{CC}		28	V
Reverse Supply Voltage	V_{RCC}		–18	V
Output Voltage	V_{OUT}		24	V
Reverse Output Voltage	V_{ROUT}		–0.5	V
Output Current	$I_{OUTSINK}$	Internal current limiting is intended to protect the device from output short circuits, but is not intended for continuous operation	25	mA
Reverse Output Current	I_{OUT}	V_{OUT} > –0.5 V, T_A = 25°C	–50	mA
Operating Ambient Temperature	T_A	L temperature range	–40 to 150	°C
Maximum Junction Temperature	T_J(max)		165	°C
Storage Temperature	T_{stg}	V_{CC} = 0 V	–65 to 170	°C

Pinout Diagram



Terminal List Table

Number	Name	Function
1	VCC	Input power supply; use bypass capacitor to connect to ground; also used for programming
2	GND	Ground
3	PWMOUT	Open drain pulse width modulated output signal

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OPERATING CHARACTERISTICS Valid over full operating temperature range, T_A, V_{CC} = 4.5 to 18 V, C_{BYPASS} = 0.1 µF, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Electrical Characteristics						
Supply Voltage	V_{CC}		4.5	–	18	V
Supply Current	I_{CC}		–	6	10	mA
Supply Zener Clamp Voltage	$V_{Zsupply}$	I_{CC} = 18 mA, T_A = 25°C, t < 5 min	28	–	–	V
Power On Time[1,2,3]	t_{PO}	f_{pwm} = 2 kHz	–	–	4	ms
Internal Bandwidth	BW_i	Small signal –3 dB, 100 $G_{(P-P)}$ magnetic input signal	–	400	–	Hz
Chopping Frequency[4]	f_C	T_A = 25°C	–	200	–	kHz
Output Characteristics						
PWMOUT Saturation Voltage	V_{SAT}	$I_{OUTSINK}$ ≤ 20 mA, PWMOUT transistor on	–	–	0.6	V
		$I_{OUTSINK}$ ≤ 10 mA, PWMOUT transistor on	–	–	0.5	V
PWMOUT Current Limit	I_{LIMIT}	R_L = 0 Ω	30	60	80	mA
PWMOUT Leakage Current	I_{LEAK}	VCC = 3.2 V, 0 V ≤ PWMOUT ≤ 24 V, PWMOUT transistor off	–	0.1	10	µA
PWMOUT Zener Clamp Voltage	V_{ZOUT}	$I_{OUTSINK}$ = I_{LIMIT}, T_A = 25°C	28	–	–	V
PWMOUT Rise Time[2,3]	t_r	R = 2 kΩ, C = 20 pF	–	3	–	µs
PWMOUT Fall Time[2,3]	t_f	R= 2 kΩ, C = 20 pF	–	3	–	µs
Maximum Propagation Delay[2,3]	$t_{pd(max)}$		–	1.5	–	ms
Response Time[2,3]	$t_{RESPONSE}$	Impulse magnetic field of 300 G, f_{pwm} = 2 kHz	–	–	2	ms
Load Resistance (External)[3]	R_L	PWMOUT to VCC	2040	–	–	Ω
Load Capacitance (External)[3]	C_L	PWMOUT to GND	–	–	10	nF
Duty Cycle Jitter[2,3,5]	J_D	Measured over 1000 output PWM clock periods, 3 sigma values, Sens = 60 m% / G	–	–	±0.090	% D
Clamp Duty Cycle[3]	$D_{CLP(HIGH)}$		90	–	95	% D
	$D_{CLP(LOW)}$		5	–	10	% D
Pre-Programming Target[6]						
Pre-Programming Quiescent Duty Cycle Output	$D_{(Q)PRE}$	B = 0 G, T_A = 25°C	–	52	–	% D
Pre-Programming Sensitivity	$Sens_{PRE}$	T_A = 25°C	–	20	–	(m% D)/G
Pre-Programming PWM Output Carrier Frequency	f_{PWMPRE}	T_A = 25°C	–	2.8	–	kHz
Quiescent Duty Cycle Programming						
Initial Quiescent Duty Cycle Output	$D_{(Q)init}$	T_A = 25°C	–	$D_{(Q)PRE}$	–	% D
Guaranteed Quiescent Duty Cycle Output Range[7]	$D_{(Q)}$	T_A = 25°C	40	–	60	% D
Quiescent Duty Cycle Output Programming Bits			–	9	–	bit
Average Quiescent Duty Cycle Output Step Size[8,9]	$Step_{D(Q)}$	T_A = 25°C	0.085	0.100	0.115	% D
Quiescent Duty Cycle Output Programming Resolution[10]	$Err_{PGD(Q)}$	T_A = 25°C	–	$Step_{D(Q)}$ × ±0. 5	–	% D

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OPERATING CHARACTERISTICS (continued) Valid over full operating temperature range, T_A, V_{CC} = 4.5 to 18 V, C_{BYPASS} = 0.1 µF, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Sensitivity Programming						
Initial Sensitivity	$Sens_{init}$	T_A = 25°C	–	$Sens_{PRE}$	–	(% D)/G
Guaranteed Sensitivity Range	$Sens_{LOW}$	T_A = 25°C	45	–	75	(m% D)/G
Sensitivity Programming Bits			–	8	–	bit
Average Sensitivity Step Size[8,9]	$Step_{SENS(low)}$	T_A = 25°C	150	300	450	(µ% D)/G
Sensitivity Programming Resolution[10]	Err_{PGSENS}	T_A = 25°C	–	$Step_{SENS}$ × ±0. 5	–	(µ% D)/G
Carrier Frequency Programming						
Initial Carrier Frequency	$f_{PWMinit}$	T_A = 25°C	–	f_{PWMPRE}	–	Hz
Carrier Frequency Programming Range	f_{PWM}	T_A = 25°C	1.8	2	2.2	kHz
Carrier Frequency Programming Bits			–	4	–	bit
Average Carrier Frequency Step Size[8,9]	$Step_{fPWM}$	T_A = 25°C	90	114	140	Hz
Carrier Frequency Programming Resolution[10]	Err_{PGfPWM}	T_A = 25°C	–	$Step_{fPWM}$ × ±0. 5	–	Hz
Calibration Test Mode						
Calibration Test Mode Duration[3]	t_{CAL}	f_{PWM} = 2 kHz	45	50	55	ms
Output Duty Cycle During Calibration Mode[3]	D_{CAL}	T_A = 25°C	49	50	51	% D
Lock Bit Programming						
Overall Programming Lock Bit	LOCK		–	1	–	bit
Factory Programmed Sensitivity Temperature Coefficient And Drift Characteristics						
Sensitivity Temperature Coefficient[11]	$Sens_{TC}$	T_A = 150°C	–	0.03	–	%/°C
Sensitivity Drift Through Temperature Range[12]	$\Delta Sens_{TC}$	T_A = 150°C	–	< ±3	–	%
Sensitivity Drift Due to Package Hysteresis[2]	$\Delta Sens_{PKG}$	T_A = 150°C, after temperature cycling	–	< ±1	–	%
Factory Programmed Duty Cycle Drift						
Duty Cycle Temperature Coefficient[11]	D_{TC}	T_A = 150°C	–	0	–	(% D)/°C
Quiescent Duty Cycle Drift Through Temperature Range	$\Delta D_{(Q)}$	Sens = $Sens_{PRE}$, T_A = 150°C	–	< ±0.35	–	% D

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Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Error Components						
Linearity Sensitivity Error[2,3]	Lin_{ERR}		–	–	±3.0	%
Symmetry Sensitivity Error[2,3]	Sym_{ERR}		–	–	±1.5	%

[1]After powering on the device, output of device needs time to reach valid magnetic response with a valid PWM output.
[2]See Characteristic Definitions section.
[3]Guarenteed by design only. Characterized but not tested in production.
[4]f_C varies up to approximately ± 20% over the full operating ambient temperature range, T_A, and process.
[5]Jitter is dependent on the sensitivity of the device.
[6]Raw device characteristic values before any programming.
[7]$D_{(Q)}$(max) is the value available with all programming fuses blown (maximum programming code set). The $D_{(Q)}$ range is the total range from $D_{(Q)}$(min) up to and including $D_{(Q)}$(max). See Characteristic Definitions section.
[8]Step size is larger than required, in order to provide for manufacturing spread. See Characteristic Definitions section.
[9]Non-ideal behavior in the programming DAC can cause the step size at each significant bit rollover code to be greater than twice the maximum specified value of $Step_{D(Q)}$, $Step_{SENS}$, or $Step_{fPWM}$.
[10]Overall programming value accuracy. See Characteristic Definitions section.
[11]Programmed at 150°C and calculated relative to 25°C.
[12]Sensitivity drift from expected value at T_A after programming $SENS_{TC}$. See Characteristic Definitions section.

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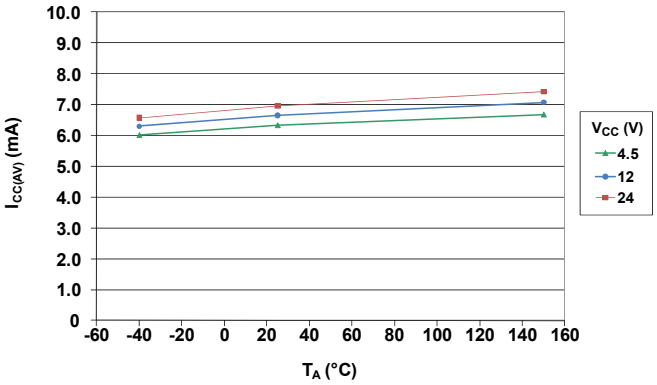
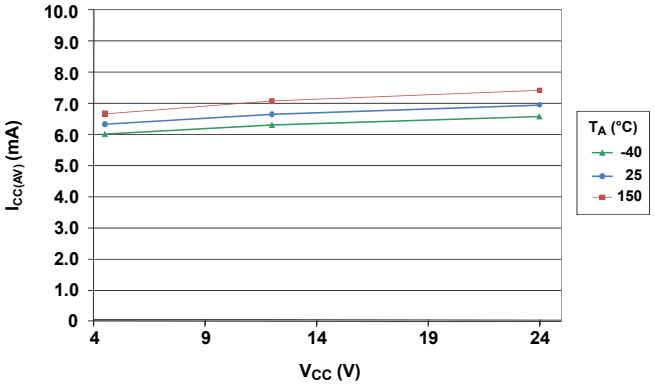
Characteristic Performance

Average Supply Current versus Temperature

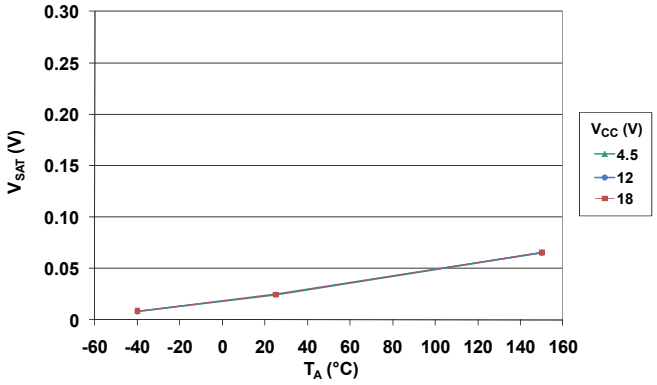


Average Supply Current versus Supply Voltage



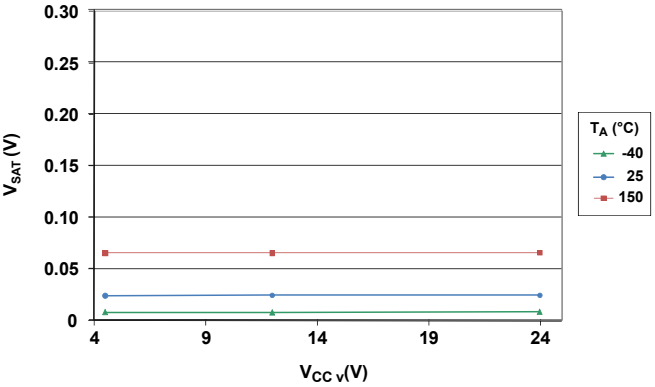
Average PWMOut Saturation Voltage versus Temperature

I_{sink} = 10 mA



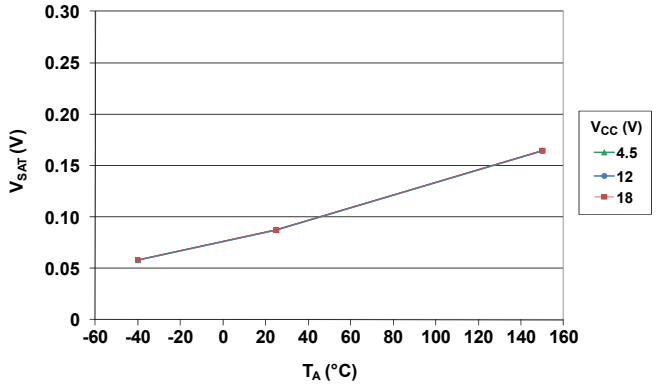
Average PWMOut Saturation Voltage versus Supply Voltage

I_{sink} = 10 mA



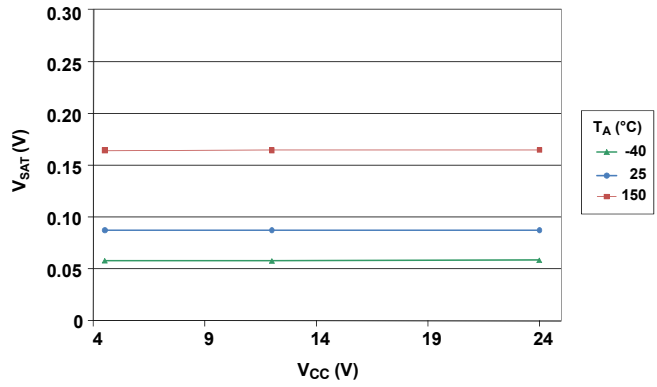
Average PWMOut Saturation Voltage versus Temperature

I_{sink} = 20 mA



Average PWMOut Saturation Voltage versus Supply Voltage

I_{sink} = 20 mA



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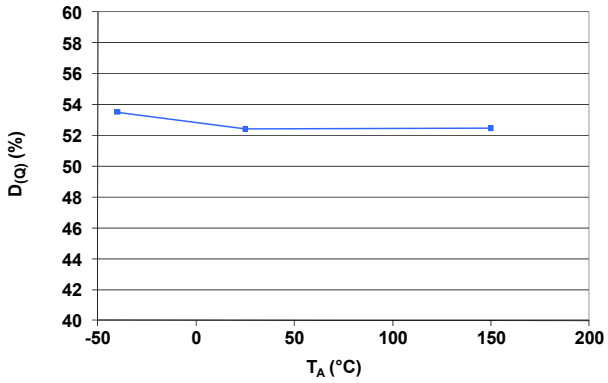
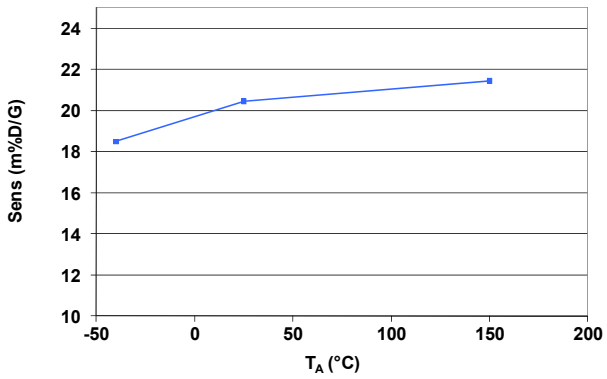
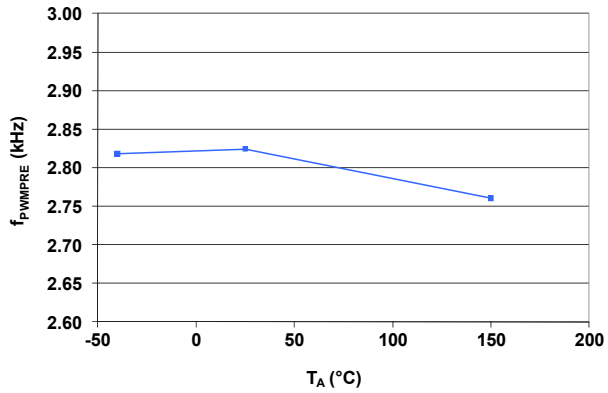
Average Pre-Programming QDC Output versus Temperature



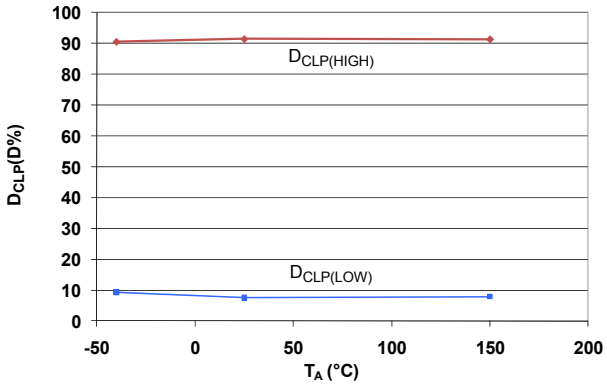
Average Pre-Programming Sensitivity versus Temperature



Average Pre-Programming PWM Output Carrier Frequency versus Temperature



Pre-Programming Clamp Duty Cycle versus Temperature



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Characteristic Definitions

Power-On Time When the supply is ramped to its operating voltage, the device requires a finite time to power its internal components before supplying a valid PWM output duty-cycle. Power-On Time, t_{PO}, is defined as the time it takes for the output voltage to settle within ±10% of its steady state value after the power supply has reached its minimum specified operating voltage, V_{CC}(min). (See figure 1.)

Propagation Delay Traveling time of signal from input Hall plate to output stage of device. (See figure 2.)

Response Time The time interval between a) when the applied magnetic field reaches 90% of its final value, and b) when the sensor IC reaches 90% of its output corresponding to the applied magnetic field. (See figure 2.)

PWM Rise Time The time elapsed between 10% and 90% of the rising signal value when output switches from low to high states.

PWM Fall Time The time elapsed between 90% and 10% of the falling signal value when output switches from high to low states.

Quiescent Duty Cycle In the quiescent state (no significant magnetic field: B = 0 G), the output duty cycle, $D_{(Q)}$, equals a specific programmed duty cycle throughout the entire operating ranges of V_{CC} and ambient temperature, T_A.

Guaranteed Quiescent Duty Cycle Output Range The Quiescent Duty Cycle Output, $D_{(Q)}$, can be programmed around its nominal value of 50% D, within the Guaranteed Quiescent Duty Cycle Range limits: $D_{(Q)}$(min) and $D_{(Q)}$(max). The available guaranteed programming range for $D_{(Q)}$ falls within the distributions of the minimum and the maximum programming code for setting $D_{(Q)}$. (See figure 3.)

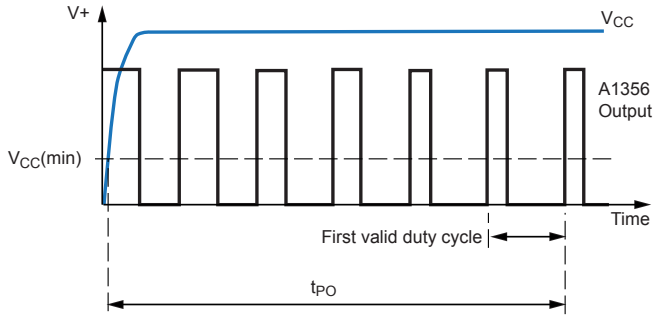

Figure 1. Definition of Power-On Time

Average Quiescent Duty Cycle Output Step Size The average quiescent duty cycle output step size for a single device is determined using the following calculation:

$$\text{Step}_{D(Q)} = \frac{D_{(Q)}(\text{max}) - D_{(Q)}(\text{min})}{2^n - 1}, \quad (1)$$

where:

n is the number of available programming bits in the trim range,

2^n-1 is the value of programming steps in the range,

$D_{(Q)}$(max) is the maximum reached quiescent duty cycle, and

$D_{(Q)}$(min) is minimum reached quiescent duty cycle.

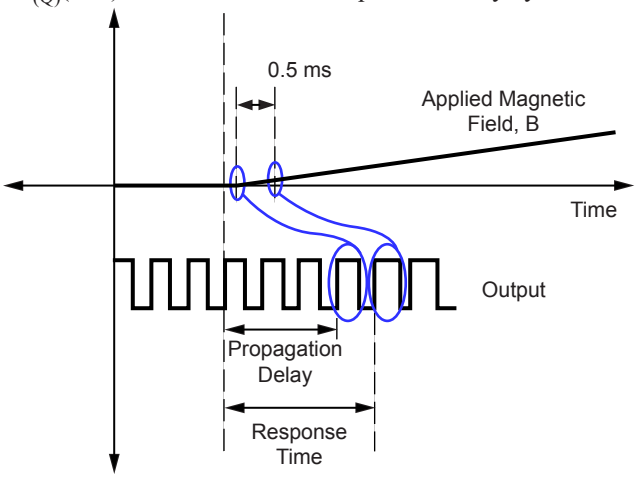

Figure 2. Definitions of Propagation Delay and Response Time

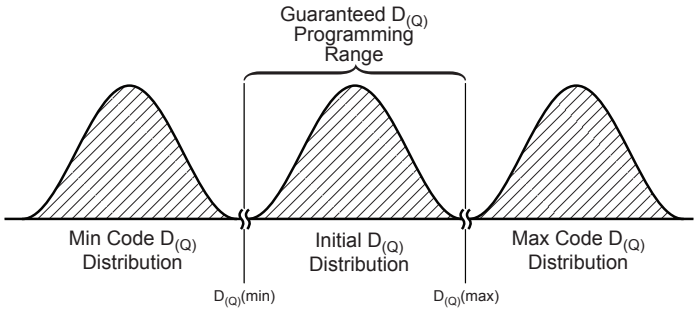

Figure 3. Definition of Guaranteed Quiescent Voltage Output Range

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Quiescent Duty Cycle Output Programming Resolution The programming resolution for any device is half of its programming step size. Therefore, the typical programming resolution will be:

$$Err_{PGD(Q)}(typ) = 0.5 \times Step_{D(Q)}(typ) \quad . \qquad (2)$$

Quiescent Duty Cycle Output Drift through Temperature Range Due to internal component tolerances and thermal considerations, the quiescent Duty Cycle Temperature Coefficient, $D_{TC}(Q)$, may drift from its nominal value over the operating ambient temperature, T_A. For purposes of specification, the Quiescent Duty Cycle Output Drift Through Temperature Range, $\Delta D_{(Q)}$ (% D), is defined as:

$$\Delta D_{(Q)} = D_{(Q)(TA)} - D_{(Q)(25°C)} \quad , \qquad (3)$$

where $D_{(Q)(TA)}$ is the quiescent duty cycle measured at T_A and is $D_{(Q)(25°C)}$ quiescent duty cycle measured at 25°C.

Sensitivity The presence of a south polarity magnetic field, perpendicular to the branded surface of the package face, increases the output duty cycle from its quiescent value toward the maximum duty cycle limit. The amount of the output duty cycle increase is proportional to the magnitude of the magnetic field applied. Conversely, the application of a north polarity field decreases the output duty cycle from its quiescent value. This proportionality is specified as the magnetic sensitivity, Sens ((% D)/G), of the device, and it is defined for bipolar devices as:

$$Sens = \frac{D_{(BPOS)} - D_{(BNEG)}}{BPOS - BNEG} \quad , \qquad (4)$$

and for unipolar devices as:

$$Sens = \frac{D_{(BPOS)} - D_{(Q)}}{BPOS} \quad , \qquad (5)$$

where BPOS and BNEG are two magnetic fields with opposite polarities.

Guaranteed Sensitivity Range The magnetic sensitivity, Sens, can be programmed around its nominal value within the sensitivity range limits: Sens(min) and Sens(max). Refer to the Guaranteed Quiescent Duty Cycle Output Range section for a conceptual explanation of how value distributions and ranges are related.

Average Sensitivity Step Size Refer to the Average Quiescent Duty Cycle Output Step Size section for a conceptual explanation.

Sensitivity Programming Resolution Refer to the Quiescent Duty Cycle Output Programming Resolution section for a conceptual explanation.

Carrier Frequency Target The PWM output signal Carrier Frequency Programming Range, f_{PWM}, can be programmed to its nominal value of 2 kHz.

Average Carrier Frequency Step Size Refer to the Average Quiescent Duty Cycle Output Step Size section for a conceptual explanation.

Carrier Frequency Programming Resolution Refer to the Quiescent Duty Cycle Output Programming Resolution section for a conceptual explanation.

Sensitivity Temperature Coefficient Device sensitivity changes as temperature changes, with respect to its programmed sensitivity temperature coefficient, $SENS_{TC}$. $SENS_{TC}$ is programmed at 150°C, and calculated relative to the nominal sensitivity programming temperature of 25°C. $SENS_{TC}$ (%/°C) is defined as:

$$Sens_{TC} = \left(\frac{Sens_{T2} - Sens_{T1}}{Sens_{T1}} \times 100\%\right)\left(\frac{1}{T2 - T1}\right) \quad , \qquad (6)$$

where T1 is the nominal Sens programming temperature of 25°C, and T2 is the programming temperature of 150°C. The expected value of Sens over the full ambient temperature range, $Sens_{EXPECTED(TA)}$, is defined as:

$$Sens_{EXPECTED(TA)} = \frac{Sens_{T1} \times [100\% + Sens_{TC}(T_A - T1)]}{100\ \%} \quad . \qquad (7)$$

$Sens_{EXPECTED\ (TA)}$ should be calculated using the actual measured values of $Sens_{T1}$ and $SENS_{TC}$ rather than programming target values.

Sensitivity Drift Through Temperature Range Second order sensitivity temperature coefficient effects cause the magnetic sensitivity, Sens, to drift from its expected value over the operating ambient temperature range, T_A. For purposes of specification, the Sensitivity Drift Through Temperature Range, $\Delta Sens_{TC}$, is defined as:

$$\Delta Sens_{TC} = \frac{Sens_{TA} - Sens_{EXPECTED(TA)}}{Sens_{EXPECTED(TA)}} \times 100\% \quad . \qquad (8)$$

Sensitivity Drift Due to Package Hysteresis Package stress and relaxation can cause the device sensitivity at $T_A = 25°C$ to change during and after temperature cycling.

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For purposes of specification, the Sensitivity Drift Due to Package Hysteresis, $\Delta Sens_{PKG}$, is defined as:

$$\Delta Sens_{PKG} = \frac{Sens_{(25°C)2} - Sens_{(25°C)1}}{Sens_{(25°C)1}} \times 100\% \quad , \tag{9}$$

where $Sens_{(25°C)1}$ is the programmed value of sensitivity at T_A = 25°C, and $Sens_{(25°C)2}$ is the value of sensitivity at T_A = 25°C, after temperature cycling T_A up to 150°C, down to –40°C, and back to up 25°C.

Linearity Sensitivity Error The A1356 is designed to provide a linear output in response to a ramping applied magnetic field. Consider two magnetic fields, B1 and B2. Ideally, the sensitivity of a device is the same for both fields, for a given supply voltage and temperature. Linearity error is present when there is a difference between the sensitivities measured at B1 and B2.

Linearity Error is calculated separately for the positive (Lin_{ERRPOS}) and negative (Lin_{ERRNEG}) applied magnetic fields. Linearity error (%) is measured and defined as:

$$Lin_{ERRPOS} = \left(1 - \frac{Sens_{BPOS2}}{Sens_{BPOS1}}\right) \times 100\% \quad ,$$

$$Lin_{ERRNEG} = \left(1 - \frac{Sens_{BNEG2}}{Sens_{BNEG1}}\right) \times 100\% \quad , \tag{10}$$

where:

$$Sens_{Bx} = \frac{|D_{(Bx)} - D_{(Q)}|}{B_x} \quad . \tag{11}$$

and B_{POSx} and B_{NEGx} are positive and negative magnetic fields, with respect to the quiescent duty cycle output such that B_{POS2} = 2 × B_{POS1} and B_{NEG2} = 2 × B_{NEG1}.

Then:

$$Lin_{ERR} = \max(Lin_{ERRPOS}, Lin_{ERRNEG}) \quad . \tag{12}$$

Note that unipolar devices only have positive linearity error (LIN_{ERRPOS}).

Symmetry Sensitivity Error The magnetic sensitivity of A1356 device is constant for any two applied magnetic fields of equal magnitude and opposite polarities. Symmetry error, Sym_{ERR} (%), is measured and defined as:

$$Sym_{ERR} = \left(1 - \frac{Sens_{BPOS}}{Sens_{BNEG}}\right) \times 100\% \quad , \tag{13}$$

where $Sens_{Bx}$ is as defined in equation 11, and BPOS and BNEG are positive and negative magnetic fields such that |BPOS| = |BNEG|. Note that the symmetry error specification is only valid for bipolar devices.

Jitter The duty cycle of the PWM output may vary slightly over time despite the presence of a constant applied magnetic field and a constant carrier frequency for the PWM signal. This phenomenon is known as jitter, and is defined as:

$$J_{DC} = \pm \frac{D_B(max) - D_B(min)}{2} \quad , \tag{14}$$

where D_B(max) and D_B(min) are the maximum and minimum duty cycles at a constant applied magnetic field, B, measured over 1000 PWM clock periods with a constant applied magnetic field. J_D is given in % D.

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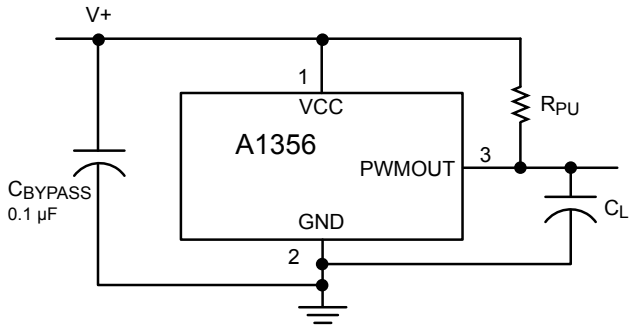
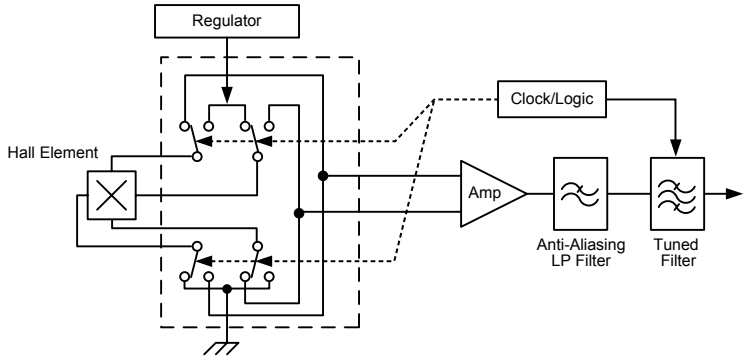
Typical Application Drawing



Chopper Stabilization Technique

When using Hall-effect technology, a limiting factor for switchpoint accuracy is the small signal voltage developed across the Hall element. This voltage is disproportionally small relative to the offset that can be produced at the output of the Hall sensor IC. This makes it difficult to process the signal while maintaining an accurate, reliable output over the specified operating temperature and voltage ranges. Chopper stabilization is a unique approach used to minimize Hall offset on the chip. Allegro employs a technique to remove key sources of the output drift induced by thermal and mechanical stresses. This offset reduction technique is based on a signal modulation-demodulation process. The undesired offset signal is separated from the magnetic field-induced signal in the frequency domain, through modulation. The subsequent demodulation acts as a modulation process for the offset, causing the magnetic field-induced signal to recover its original spectrum at base band, while the DC offset becomes a high-frequency signal. The magnetic-sourced signal then can pass through a low-pass filter, while the modulated DC offset is suppressed. In addition to the removal of the thermal and stress related offset, this novel technique also reduces the amount of thermal noise in the Hall sensor IC while completely removing the modulated residue resulting from the chopper operation. The chopper stabilization technique uses a high-frequency sampling clock. For the demodulation process, a sample-and-hold technique is used. This high-frequency operation allows a greater sampling rate, which results in higher accuracy and faster signal-processing capability. This approach desensitizes the chip to the effects of thermal and mechanical stresses, and produces devices that have extremely stable quiescent Hall output voltages and precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process, which allows the use of low-offset, low-noise amplifiers in combination with high-density logic integration and sample-and-hold circuits.



Chopper Stabilization Technique

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Programming Guidelines

OVERVIEW

Programming is accomplished by sending a series of input voltage pulses serially through the VCC pin of the device. A unique combination of different voltage level pulses controls the internal programming logic of the device to select a desired programmable parameter and change its value. There are three voltage levels that must be taken into account when programming. These levels are referred to as *high*, $V_{P(HIGH)}$, *mid*, $V_{P(MID)}$, and low, $V_{P(LOW)}$.

The 1356 features Try mode, Blow mode and Lock mode:

- In Try mode, the value of multiple programmable parameters may be set and measured simultaneously. The parameter values are stored temporarily, and reset after cycling the supply voltage.
- In Blow mode, the value of a single programmable parameter may be set and measured, and then permanently set by blowing solid-state fuses internal to the device. Additional parameters may be blown sequentially. This mode also is used for blowing the device-level fuse (when Lock mode is enabled), which permanently blocks the further programming of all parameters.
- Lock mode prevents all future programming of the device. This is accomplished by blowing a special fuse using Blow mode.

The programming sequence is designed to help prevent the device from being programmed accidentally; for example, as a result of noise on the supply line. Although any programmable variable power supply can be used to generate the pulse waveforms, Allegro highly recommends using the Allegro Sensor Evaluation Kit, available on the Allegro website On-line Store. The manual for that kit is available for download free of charge, and provides additional information on programming these devices.

DEFINITION OF TERMS

Register The section of the programming logic that controls the choice of programmable modes and parameters.

Bit Field The internal fuses unique to each register, represented as a binary number. Changing the bit field settings of a particular register causes its programmable parameter to change, based on the internal programming logic.

Key A series of mid-level voltage pulses used to select a register, with a value expressed as the decimal equivalent of the binary value. The LSB of a register is denoted as key 1, or bit 0.

Code The number used to identify the combination of fuses activated in a bit field, expressed as the decimal equivalent of the binary value. The LSB of a bit field is denoted as code 1, or bit 0.

Addressing Increasing the bit field code of a selected register by serially applying a pulse train through the VCC pin of the device. Each parameter can be measured during the addressing process, but the internal fuses must be blown before the programming code (and parameter value) becomes permanent.

Fuse Blowing Applying a high voltage pulse of sufficient duration to permanently set an addressed bit by blowing a fuse internal to the device. After a bit (fuse) has been blown, it cannot be reset.

Blow Pulse A high voltage pulse of sufficient duration to blow the addressed fuse.

Cycling the Supply Powering-down, and then powering-up the supply voltage. Cycling the supply is used to clear the programming settings in Try mode.

Programming Pulse Requirements, Protocol at T_A = 25 °C

Characteristic	Symbol	Notes	Min.	Typ.	Max.	Unit
Programming Voltage	$V_{P(LOW)}$	Measured at the VCC pin.	–	5	5.5	V
	$V_{P(MID)}$		13	15	16	V
	$V_{P(HIGH)}$		26	27	28	V
Programming Current	I_P	Minimum supply current required to ensure proper fuse blowing. In addition, a minimum capacitance, C_{BLOW} = 0.1 µF, must be connected between the supply and GND pins during programming to provide the current necessary for fuse blowing. The blowing capacitor should be removed and the load capacitance used for properly programming duty cycle measurements.	300	–	–	mA
Pulse Width	t_{LOW}	Duration of $V_{P(LOW)}$ for separating $V_{P(MID)}$ and $V_{P(HIGH)}$ pulses.	40	–	–	µs
	t_{ACTIVE}	Duration of $V_{P(MID)}$ and $V_{P(HIGH)}$ pulses for register selection or bit field addressing.	40	–	–	µs
	t_{BLOW}	Duration of $V_{P(HIGH)}$ pulses for fuse blowing.	40	–	–	µs
Pulse Rise Time	t_{Pr}	Rise time required for transitions from $V_{P(LOW)}$ to either $V_{P(MID)}$ or $V_{P(HIGH)}$.	5	–	100	µs
Pulse Fall Time	t_{Pf}	Fall time required for transitions from $V_{P(HIGH)}$ to either $V_{P(MID)}$ or $V_{P(LOW)}$.	5	–	100	µs

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Programming Procedures

MODE AND PARAMETER SELECTION

Each programmable mode and parameter can be accessed through specific registers. To select a register, a sequence of voltage pulses consisting of a $V_{P(HIGH)}$ pulse, a series of $V_{P(MID)}$ pulses, and a $V_{P(HIGH)}$ pulse (with no VCC supply interruptions) must be applied serially to the supply pin. The quantity of $V_{P(MID)}$ pulses is called the key, and uniquely identifies each register. The pulse train used for selection of the first register, key 1, is shown in figure 4.

The A1356 has two registers that select among the three programmable modes:

- Register Mode 1:

  Blow and Lock modes

- Register Mode 2:

  Try mode

And there are four registers that select among the four programmable parameters:

- Register 1:

  Sensitivity, Sens

- Register 2:

  Quiescent duty cycle output, $D_{(Q)}$

- Register 3:

  Pulse width modulated carrier frequency , f_{PWM}

- Register 5:

  Lock (device locking)

BIT FIELD ADDRESSING

After a programmable parameter has been selected, a $V_{P(HIGH)}$ pulse transitions the programming logic into the bit field addressing state. Applying a series of $V_{P(MID)}$ pulses to the VCC pin of the device, as shown in figure 5, increments the bit field of the selected parameter.

When addressing the bit field, the number of $V_{P(MID)}$ pulses is represented by a decimal number called a *code*. Addressing activates the corresponding fuse locations in the given bit field by increasing the binary value of an internal DAC. The value of the bit field (and code) increases by one with the falling edge of each $V_{P(MID)}$ pulse, up to the maximum possible code (see the Programming Logic table). As the value of the bit field code increases, the value of the programmable parameter changes. Measurements can be taken after each pulse to determine if the required result for the programmable parameter has been reached. Cycling the supply voltage resets all the locations in the bit field that have unblown fuses to their initial states.

FUSE BLOWING

After the required code is found for a given parameter, its value can be set permanently by blowing individual fuses in the appropriate register bit field. Blowing is accomplished by applying a $V_{P(HIGH)}$ pulse, called a *blow* pulse, of sufficient duration at the $V_{P(HIGH)}$ level to permanently set an addressed bit by blowing a fuse internal to the device. Due to power requirements, the fuse for each bit in the bit field must be blown individually. To accomplish this, the code representing the required parameter value must be translated to a binary number. For example, as shown in figure 6, decimal code 5 is equivalent to the binary number 101. Therefore bit 2 (code 4) must be addressed and blown, the device power supply cycled, and then bit 0 (code 1) addressed

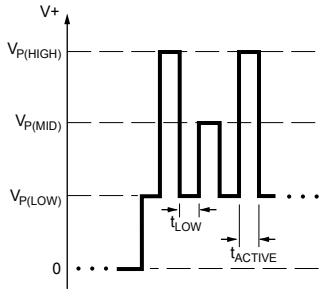

Figure 4. Parameter selection pulse train. This shows the sequence for selecting the register corresponding to key 1, indicated by a single $V_{P(MID)}$ pulse.

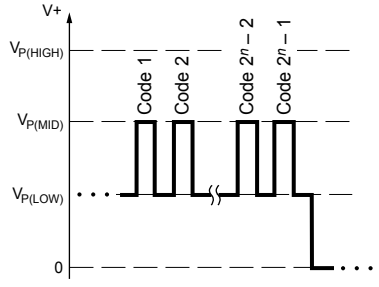

Figure 5. Bit field addressing pulse train. Addressing the bit field by increasing the code causes the programmable parameter value to change. The number of bits available for a given programming code, *n*, varies among parameters; for example, the bit field for $D_{(Q)}$ has 8 bits available, which allows 255 separate codes to be used.

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and blown. An appropriate sequence for blowing code 5 is shown in figure 7. The order of blowing bits, however, is not important. Blowing bit 0 first, and then bit 2 is acceptable.

Note: After blowing, the programming is not reversible, even after cycling the supply power. Although a register bit field fuse cannot be reset after it is blown, additional bits within the same register can be blown at any time until the device is locked. For example, if bit 1 (binary 10) has been blown, it is still possible to blow bit 0. The end result would be binary 11 (decimal code 3).

LOCKING THE DEVICE

After the desired code for each parameter is programmed, the device can be locked to prevent further programming of any parameters.

ADDITIONAL GUIDELINES

The additional guidelines in this section should be followed to ensure the proper behavior of these devices:

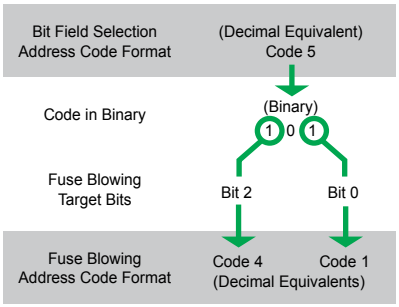

Figure 6. Example of code 5 broken into its binary components, which are code 4 and code 1.

- A 0.1 µF blowing capacitor, C_{BLOW}, must be mounted between the supply pin and the GND pin during programming, to ensure enough current is available to blow fuses.
- The application capacitance, C_L, should be used when measuring the output duty cycle during programming.
- The power supply used for programming must be capable of delivering at least 26 V and 300 mA.
- Be careful to observe the t_{LOW} delay time before powering down the device after blowing each bit.
- The following programming order is recommended:

  1. f_{PWM}
  2. Sens
  3. $D_{(Q)}$
  4. Lock the device (only after all other parameters have been programmed and validated, because this prevents any further programming of the device)

PROGRAMMING MODES

Try Mode Try mode allows multiple programmable parameters to be tested simultaneously without permanently setting any values. In this mode, each $V_{P(HIGH)}$ pulse will indefinitely loop the programming logic through the mode, register, and bit field selection states.

After powering the V_{CC} supply, select mode key 2, the desired parameter register, and address its bit field. When addressing the bit field, each $V_{P(MID)}$ pulse increments the value of the parameter register up to the maximum possible code (see Programming Logic section). The addressed parameter value is stored in the device even after the programming drive voltage is removed from

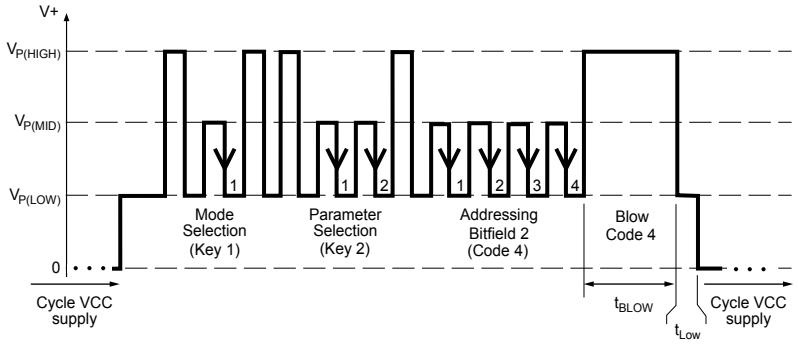

Figure 7. Example of Blow Mode programming pulses applied to the VCC pin. In this example, DC(Q) (Parameter Key 2) is addressed to code 4 (i.e bit 2) and its value is permanently blown.

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the VCC pin, allowing its value to be measured. To test an additional programmable parameter in conjunction with the original, enter an additional $V_{P(HIGH)}$ pulse on the VCC pin to reenter the parameter selection field. Select a different parameter register, and address its bit field, without any supply interruptions. Both parameter values will be stored and can be measured after removing the programming drive voltage. Multiple programming combinations can be tested to achieve optimal application accuracy. See figure 8 for an example of the Try mode pulse train.

Registers can be addressed and re-addressed an indefinite number of times in any order. After the required code is found for each register, cycle the supply and blow the bit field using Blow mode.

Blow Mode After the required value of the programmable parameter is found using Try mode, its corresponding code should be blown to make its value permanent. To do this, select the required parameter register, and address and blow each required bit separately (as described in the Fuse Blowing section). The supply must be cycled between blowing each bit of a given code. After a bit is blown, cycling the supply will not reset its value.

Single parameters can be still addressed in the Blow mode before fuse blowing. Simultaneous addressing of multiple parameters, as in Try mode, is not possible. After powering the V_{CC} supply, select the desired parameter register and address its bit field. When addressing the bit field, each $V_{P(MID)}$ pulse increments the value of the parameter register, up to the maximum possible code (see Programming Logic table). The addressed parameter value is stored in the device even after the programming drive voltage is removed from the VCC pin, allowing its value to be measured. It is not possible to decrease the value of the register without resetting the parameter bit field. To reset the bit field, and thus the value of the programmable parameter, cycle the supply, V_{CC}, voltage.

It is possible to switch between Try and Blow modes, in that after individual programmable parameters have been blown in Blow mode, other parameters can be still tested in Try mode.

Lock Mode To lock the device, address the Lock bit and apply a blow pulse with C_{BLOW} in place. After locking the device, no future programming of any parameter is possible.

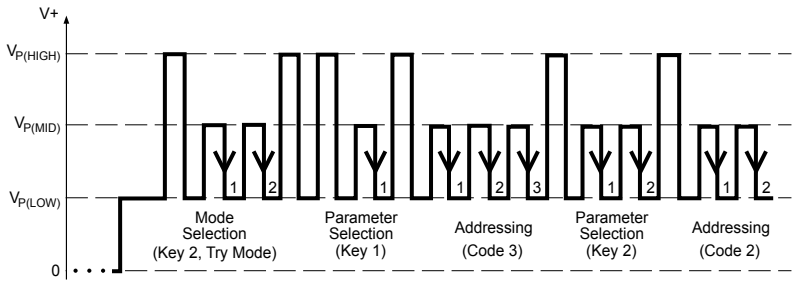

Figure 8. Example of Try mode programming pulses applied to the VCC pin. In this example, Sensitivity (parameter key 1) is addressed to code 3, and $D_{(Q)}$ (parameter key 2) is addressed to code 2. The values set in the Sensitivity and $D_{(Q)}$ registers will be held in the device until the supply is cycled. Permanent fuse blowing cannot be accomplished in Try mode.

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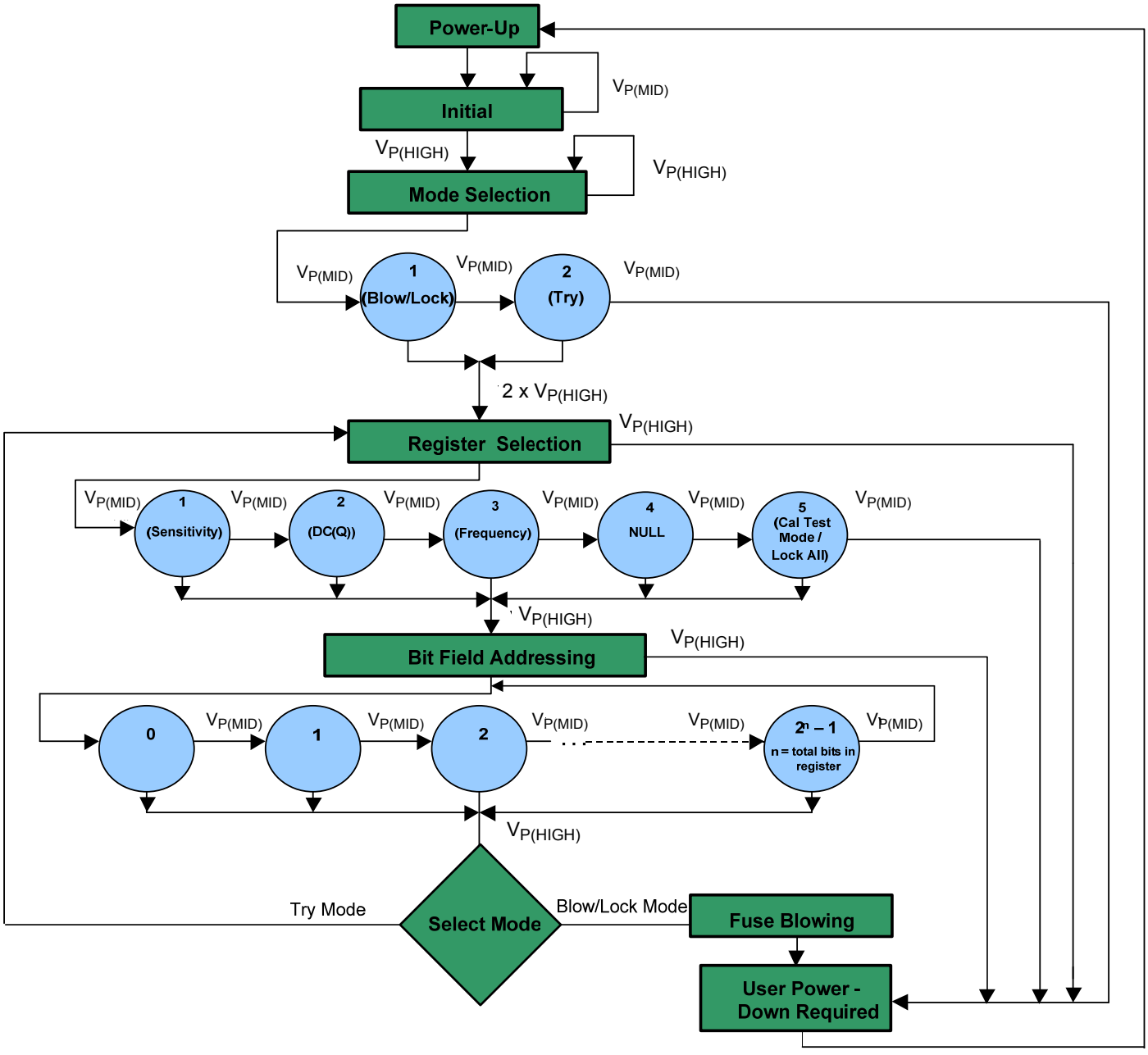
Programming State Machine



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Programming Logic Table

Mode or Parameter Name (Register Key)	Bit Field Address		Description
	Binary Format [MSB → LSB]	Decimal Equivalent Code	
Programmable Mode			
Blow, Lock (1)	01	1	Blow parameter bit field fuse
			Blow Lock fuse to lock device
Try (2)	10	2	Try code
Programmable Parameter			
Sensitivity (1)	000000000	0	Initial value, Sens = $Sens_{PRE}$
	011111111	255	Maximum Sens value in range
$D_{(Q)}$ (2)	000000000	0	Initial value, $D_{(Q)} = D_{(Q)PRE}$
	011111111	255	Maximum quiescent duty cycle in range
	100000000	256	Switch from programming increasing $D_{(Q)}$ to programming decreasing $D_{(Q)}$
	111111111	511	Minimum quiescent duty cycle in range
PWM Frequency (3)	000000000	0	Initial value; $f_{PWM} = f_{PWMPRE}$
	000001111	15	Minimum PWM frequency in range
Calibration Test Mode, Lock (5)	000000000	0	Initial value
	000010000	16	Enable Output Calibration Test Mode
	1000000000	512	Enable blowing Lock fuse to lock device

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Output Calibration Test Mode

In customer applications, the PWM interface circuitry (body control module; *BCM* in figure 9) and the A1356 may be powered via different power and ground circuits. As a result, the ground reference for the A1356 may differ from the ground reference of the BCM. In some customer applications this ground difference can be as large as ± 0.5 V. Differences in the ground reference for the A1356 and the BCM can result in variations in the threshold voltage used to measure the duty cycle of the A1356. If the PWM conversion threshold voltage varies, then the duty cycle will vary because there is a finite rise time (t_r) and fall time (t_f) in the PWM waveform. This problem is shown in figure 10. The A1356 Output Calibration mode is used to compensate for this error in the duty cycle. While the A1356 is in Output Calibration mode, the device output waveform is a fixed 50% duty cycle (the programmed quiescent duty cycle value) regardless of the applied external magnetic field. After powering-up, the A1356 outputs its quiescent duty cycle waveform for 50 ms, regardless of the applied magnetic field (see figure 11). This allows the BCM to compare the measured quiescent duty cycle with an ideal 50% duty cycle. This test period allows end users to compensate for any threshold errors that result from a difference in system ground potentials.

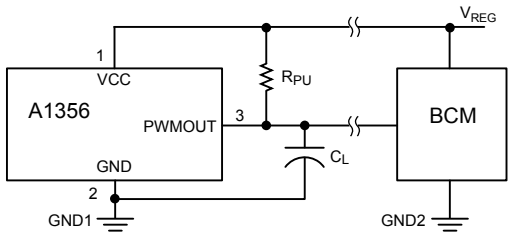

Figure 9. In many applications the A1356 may be powered using a different ground reference than the BCM. This may cause the ground reference for the A1356 (GND 1) to differ from the ground reference of the BCM (GND 2) by as much as to ± 0.5 V.

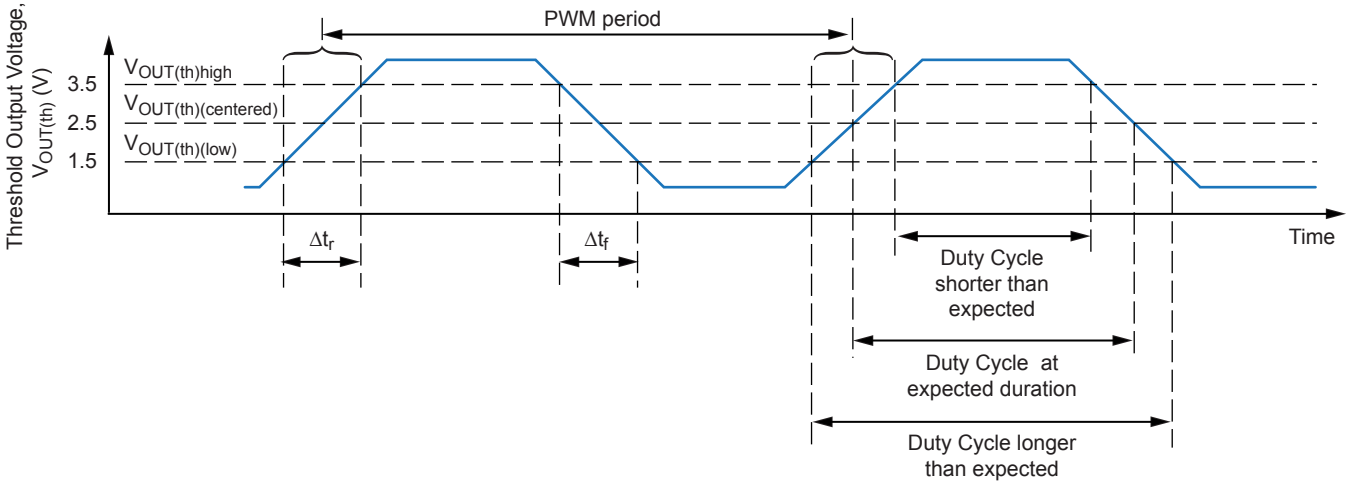

Figure 10. When the threshold voltage, $V_{OUT(th)}$, is correctly centered between , $V_{OUT(th)high}$ and , $V_{OUT(th)low}$, the duty cycle accurately coincides with the applied magnetic field. If the threshold voltage is raised, the output duty cycle appears shorter than expected. Conversely, if the threshold voltage is lowered, the output duty cycle is longer than expected.

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After the initial 50 ms has elapsed, the duty cycle will correspond to an applied magnetic field as expected. The 50 ms calibration test time corresponds with a target PWM frequency of 2 kHz. If the PWM frequency is programmed away from its target of 2 kHz, the duration of the calibration test time will scale inversely with the change in PWM frequency.

This test mode is optional and must be enabled by blowing its programming bit. After the test mode bit has been blown, the device enters Output Calibration mode every time the device is powered-on. This test mode is provided so that the user can compensate for differences in the ground potential between the A1356 and any interface circuitry used to measure the pulse width of the A1356 output.

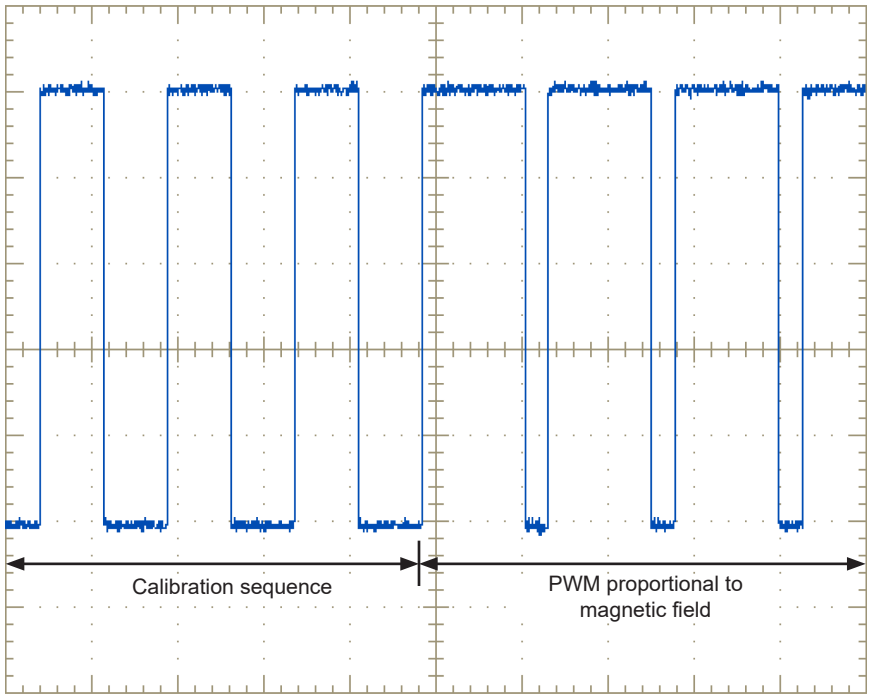

Figure 11. After powering-on, the A1356 outputs a 50% DC for the first 50 ms, regardless of the applied magnetic field (Output Calibration mode in effect). After the initial 50 ms has elapsed, the output responds to a magnetic field as expected. The example in this figure assumes that a large +B field is applied to the device after the initial 50 ms.

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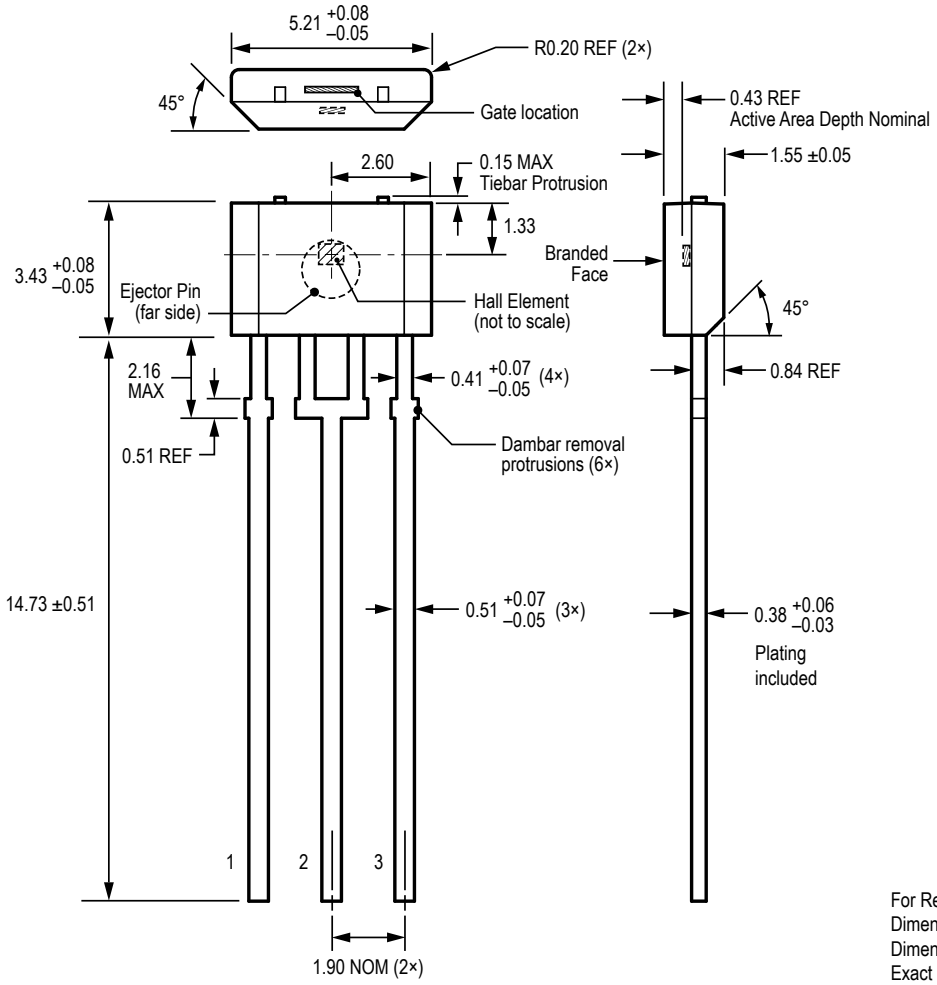
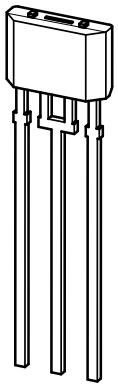
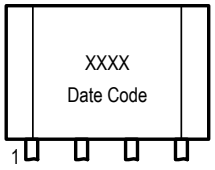
Package KB, 3-Pin SIP







Standard Branding Reference View

Lines 1, 2 = 4 characters.

Line 1: Part Number
Line 2: 4-digit Date Code

Branding scale and appearance at supplier discretion

For Reference Only; not for tooling use (reference Allegro DWG-0000225)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

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Revision History

Number	Date	Description
–	April 13, 2013	Initial release
1	February 19, 2019	Minor editorial updates
2	April 24, 2019	Updated selection guide (page 2)
3	June 14, 2021	Updated Package Outline Drawing (page 20)
4	June 22, 2022	Updated product status to Not for New Design

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