ACS37600 REFERENCE PCB DESIGN FOR CURRENT SENSING MODULE APPLICATIONS

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INTRODUCTION

This reference design incorporates the ACS37600 Hall-Effect Current Sensor IC for high-current applications with a magnetic concentrator. The aim of this document is to provide guidelines for designing a PCB for the ACS37600 while minimizing possible undershoots/overshoots due to a fast current step response. More information about the features and benefits of the ACS37600 can be found in the device datasheet. Also see Guidelines for Designing a Concentrator for High-Current Sensing Applications with an Allegro Hall-Effect Sensor IC [1] and the Interactive Core Design Tool [2] from Allegro's Software Portal.

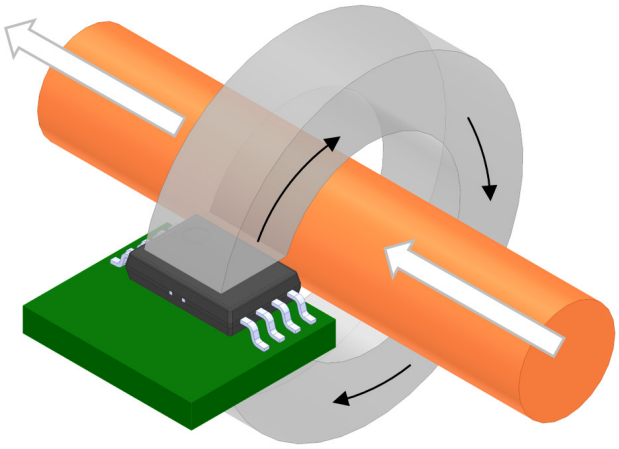

Figure 1: Typical construction of a sensing solution with a ferromagnetic core around a current carrying conductor.

PINOUT DIAGRAM AND TERMINAL LIST

Table 1: ACS37600 Terminal list

Pin Number	Name	Description
6, 7	GND, NC	Not Connected or Ground
1, 4	GND	Device Ground
5	VCC	Device Supply
2	VOUT	Device Analog Output
3	VREF	Reference Voltage
8	OCF	Over Current Fault

Pin 1 is the primary device ground and must always be connected. Pins 4, 6, and 7 are internally connected to pin 1 via the device ESD GND ring and can be left floating.

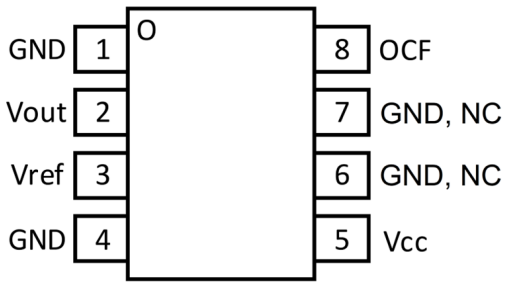

Figure 2: ACS37600 Pinout Diagram

[1] https://www.allegromicro.com/en/Insights-and-Innovations/Technical-Documents/Hall-Effect-Sensor-IC-Publications/Current-Sensor-Concentrator.

[2] https://registration.allegromicro.com/downloads/A1367%2FpartSupportFile%2FCore Design Tool v1.0.1.zip.

PACKAGE FOOTPRINT

A standard TSSOP-8 IPC-compliant footprint is recommended (Reference MO-153AA).

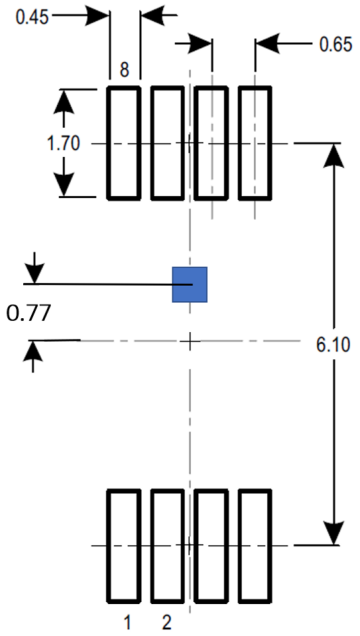

Figure 3: TSSOP-8 package footprint with Hall element location (blue square, size not in scale)

HIGH-SPEED STEP RESPONSE

Core-based sensors can be exposed to large *dΦ/dt* during a current step response such as a short circuit or in fast switching applications.

The voltage induced in a closed loop is proportional to the rate of change of magnetic flux linking the loop as defined by Faraday's law of induction. Thus, a rapid change in magnetic field through a loop creates a voltage potential with a transfer function *V = f(B)* as defined by the following formula:

$$V = -n \cdot \frac{d\Phi}{dt} = -n \cdot A \cdot \frac{dB}{dt}$$

Where Φ is the magnetic flux passing through a coil in weber, B is the magnetic flux density in tesla, A is a loop area in m^2, n is number of turns, and t is the time it takes to change Φ in seconds.

RECOMMENDED PCB LAYOUT

In order to mitigate possible undershoots/overshoots observed on the analog output of the IC, it is necessary to pay special attention to the board layout.

Positive performance has been verified with Evaluation Board ASEK37600-EVB (TED-0003124-R1) with a routing pattern shown in Figure 4.

The following loop areas are always important to minimize to avoid magnetic induction:

- VREF to GND
- VREF to VOUT
- VOUT to GND

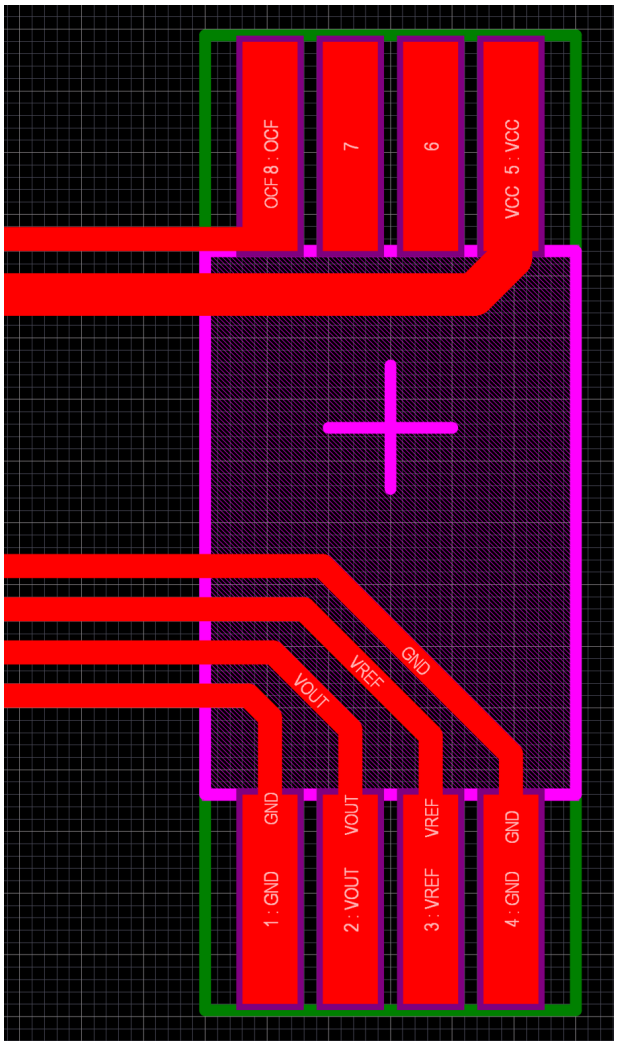

Figure 4: Recommended PCB routing

LAYOUT DETAILS

Looking at Figure 4, the purple cross indicates the position of the Hall element. It is recommended not to route any tracks / current-carrying traces in this space. The purple rectangle represents the package leadframe size (4.4 mm × 3.0 mm).

Further, the trace spacing between VREF, VOUT, and GND should be as small as the layout rules allow, ideally routed as a differential pair and shielded by GND.

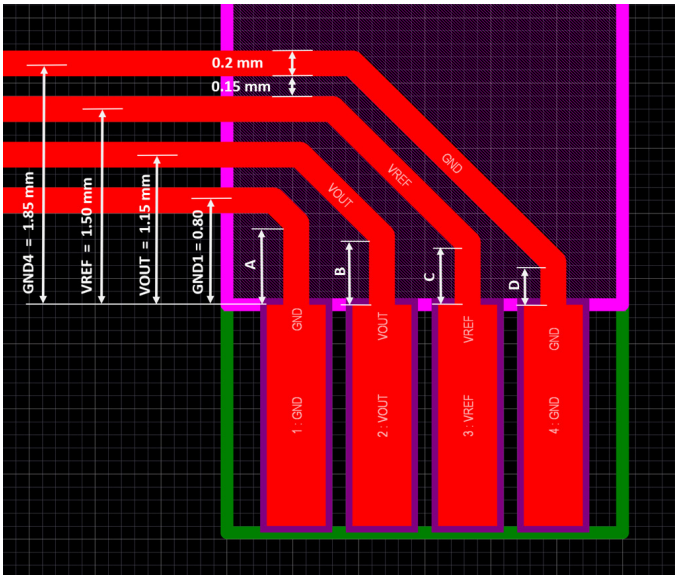

Figure 5: Detail of recommended PCB routing

COORDINATES FROM FIGURE 5

- Track width = 200 µm
- Track spacing = 150 µm
- Track center to leadframe:
  - GND4 = 1.85 mm
  - VREF = 1.50 mm
  - VOUT = 1.15 mm
  - GND1 = 0.80 mm
- Distance of first 45 degree turning:
  - A = 0.575 mm
  - B = 0.475 mm
  - C = 0.325 mm
  - D = 0.175 mm

DISCLAIMER

Overall performance shall vary depending on mechanical module design and how fast and large *dΦ/dt* input is. Allegro cannot guarantee the absolute amount of overshoot/undershoot.

Actual performance must be confirmed by customer's evaluation for each current sensor module.

Revision History

Number	Date	Description	Responsibility
–	July 29, 2020	Initial release	Radek Krystian

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